DESIGN AND OPTIMIZATION OF A LOW NOISE 2.4GHZ CMOS VCO WITH INTEGRATED LC TANK AND MOSCAP TUNING

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ABSTRACT

A 2.4GHz LC voltage controlled oscillator is designed and optimized via linear programming and implemented in a $0.35\mu m$ RF BiCMOS process technology. Our design methodology provides an insight into choosing design variables with several constraints such as voltage swing, tuning range, and start-up condition. The on-chip spiral inductors used are modeled and optimized by a $3D$ inductor simulator. The inversion mode MOSCAP tuning is used to achieve 26% of tuning range. The measured phase noise is -121dBc/Hz, -117dBc/Hz and -115dBc/Hz at 600kHz offset from 1.91GHz, 2.03GHz and 2.60GHz carriers, respectively. The VCO dissipates only 4mA from a 2.5V supply voltage.

1. INTRODUCTION

Voltage controlled oscillators are essential building blocks in communication systems and are used as local oscillators to up- and down-convert signals. Design of integrated oscillators has posed many challenges to circuit designers as it involves simultaneous optimization of multiple variables. This paper investigates a simple, yet effective, method to design and optimize integrated voltage controlled oscillators, which is suitable for both hand calculations and computer simulations. It is shown that a design method for optimization of VCOs does exist as opposed to pure, time-intensive simulation.

The cross-coupled transistor topology depicted in Fig. 1 is used as the design topology for several reasons. Full exploitation of differential operation mitigates undesirable common-mode effects, such as extrinsic substrate and supply noise. The oscillation amplitude of this structure is a factor of two larger than that of the NMOS-only structure due to the PMOS pair, which results in a better phase noise performance for a given tail current. The rise and fall time symmetry is incorporated to further reduce the *1/f* noise upconversion [1].

The design and optimization methodology is linear programming. Before performing the linear programming, the spiral inductor structure is selected so that the quality factor can be maximized for a given inductance (2.7nH) and frequency (2.4GHz). This optimal spiral structure results in higher voltage swing and lower phase noise. Constraints on voltage swing, frequency tuning range, and start-up conditions are imposed. Under these constraints, design variables are selected in such a manner that the phase noise can be minimized via linear programming. Our design methodology predicts a phase noise of -120dBc/Hz at 600kHz offset from a 2.22GHz carrier for a VCO dissipating 4mA from a 2.5V supply in simulation and is a less complicated alternative to the geometric programming introduced in [2] and [3]. It can provide more design insight as discussed in the subsequent sections.

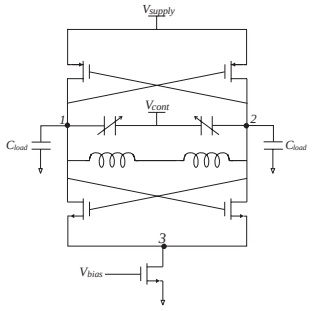

Figure 1: VCO schematic

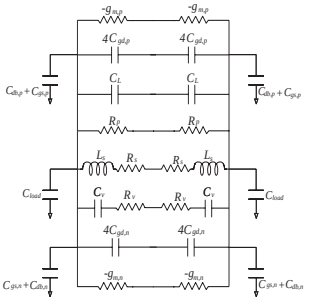

Figure 2: Tank model

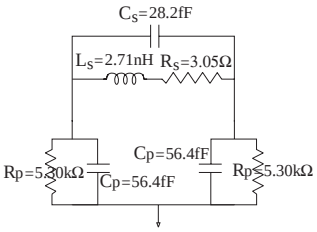

Figure 3: Sym. L model

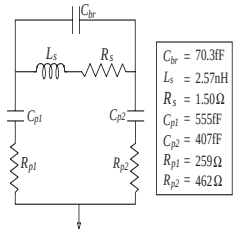

Figure 4: Asym. L model

In Section 2, building blocks of the oscillator are analyzed to derive important parameters to be used in linear programming. Section 3 explains the detail of our design procedure via linear programming. In Section 4, elaborate simulation results are presented and compared to hand-calculations. Section 5 discusses the experimental results.

2. BUILDING BLOCKS AND PARAMETERS

In this section, we analyze the building blocks of the oscillator to derive parameters for the equivalent circuit model shown in Fig. 2 [2]. These parameters will be used for the linear programming in the next section.

The VCO is implemented in Conexant's $0.35\mu m$ BiCMOS process technology, only using CMOS transistors. The transconductance, g_m, is approximated by $g_m = \mu C_{ox} W E_{sat}/2$ from the deep short-channel current-voltage expression. In our process technology, $g_{mn} = 155 W_n[\mho]$ and $g_{mp} = 48 W_p[\mho]$. The output conductance, g_d, can be approximated by $g_d = \lambda I^{0.6} L^{-1} W^{0.4}$ where λ is a fitting parameter [4].

The geometric parameters of the spiral inductors are chosen to maximize the quality factor, Q_L, for a given inductance $(2.7nH)$ in a $3D$ inductor simulator, *ASITIC* [5]. The inductor is built in the top metal layer of a three metal layer process and a Q_L of approximately 8.9 was achieved at $2.4GHz$.

Two different analytical models were developed for the inductor used. One is the symmetric model of Fig. 3 [6], which is used for linear programming. In this model, the ef-

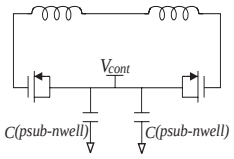

Figure 5: LC tank

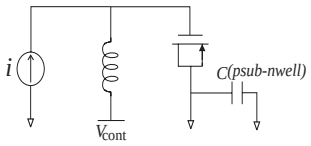

Figure 6: ac analysis

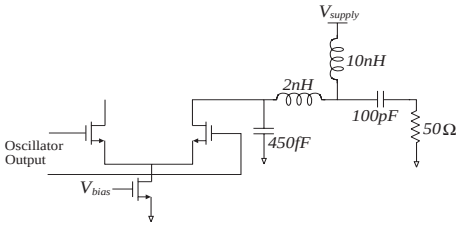

Figure 7: Output driver and measurement structure

fective parallel equivalent conductance of the inductors, g_L, is given by $1/R_p + R_s/(L\omega)^2$ [3]. The other is a more accurate non-symmetric model depicted in Fig. 4 and is used in simulations. This non-symmetric model was developed using *ASITIC* and *HSPICE* optimizers to address the physical asymmetry of the spiral structure mainly due to the metal underpass [5].

The varactors are made out of the gate channel capacitance of PMOS transistors in inversion mode. The drain and source are tied to the control node as shown in Fig. 5. The n-well is connected to the same node to reduce the effect of the junction capacitance between drain(source) and n-well. The n-well p-substrate junction capacitance appears as common mode as shown in Fig. 5 and does not affect the tuning range. The drain and source regions expedite the inversion process by supplying enough charged carriers.

The varactors of Fig. 5 show a quality factor, Q_v of 30 and C_{max}/C_{min} ratio of 2.93 in *HSPICE* ac analysis performed on the circuit of Fig. 6. The ac analysis is small-signal and does not account for nonlinear variations. Therefore, it can only be used as a starting point for the design. The effective parallel varactor conductance, $g_v = (C_v\omega)/Q_v$, can be calculated from the equivalent circuit of Fig. 6.

The tank conductance, inductance, and capacitance are given by $2G_{tank} = g_{dn} + g_{dp} + g_v + g_L$, $L_{tank} = 2L$ and $2C_{tank} = 4C_{gd,n} + C_{gs,n} + C_{db,n} + 4C_{gd,p} + C_{gs,p} + C_{db,p} + C_L + C_v + C_{load}$, respectively.

3. DESIGN OF THE OSCILLATOR TANK VIA LINEAR PROGRAMMING

The oscillator is designed to draw a maximum of 4mA of current from a 2.5V supply. The inductor is chosen based on the discussion in the previous section. Both channel-length L_n and L_p of MOSFETs are set to be the minimum (*i.e.*, 0.35 μm) to reduce parasitic capacitances. A symmetric tank ($g_{mn} = g_{mp}$) is used to improve the $1/f^3$ corner of phase noise [1] and we set $g_{mn} = g_{mp}$ or, $W_p = 3.23W_n$. The MOSCAP involves one design variable, $C_{v,max}$, while $C_{v,min} = 0.34C_{v,max}$ from the MOSCAP ac analysis. The output driver adds about 60fF of load capacitance to the tank. Consequently, we have three design variables to optimize: W_n, $C_{v,max}$, and I.

3.1. Constraints

We specify a minimum voltage swing of 2V from 2.5V voltage supply, *i.e.*, $V_{sw} = I/G_{tank,max} \geq 2$ where $G_{tank,max}$ imposes the worst-case constraint. Note this constraint is valid only in the current-limited regime [1].

We specify a tuning range in excess of 15%. With a center frequency of 2.4GHz, the frequency should change at least from $f_{min} = 2.22GHz$ to $f_{max} = 2.58GHz$, which implies $L_{tank}C_{tank,min} \leq \omega_{max}^{-2}$ and $L_{tank}C_{tank,max} \geq \omega_{min}^{-2}$.

We impose a rather conservative start-up condition with a loop gain of at least 3, hence $g_{mn} \geq \alpha_g G_{tank,max}$ and $\alpha_g \geq 3$, which reduces to $3G_{tank,max}/g_{mn} \leq 1$ where the worst-case condition is imposed by $G_{tank,max}$.

The size of the output driver transistors in Fig. 7 is chosen so that it can drive a 50Ω load at 0dBm with the 2V of input voltage swing. This results in an output differential pair with a W/L of $40\mu m/0.35\ \mu m$ which will load the oscillator core by $C_{load} \sim 60fF$. Since this capacitance is only 4% of the varactor capacitance obtained in the following section, reasonable change in the transistor width negligibly affects the tuning range constraints. The voltage swing and start-up constraints are not affected by the load capacitance.

3.2. Phase Noise

The phase noise in the $1/f^2$ region is given by [1]

$$\mathcal{L}\{f_{off}\} = \frac{1}{8\pi^2 f_{off}^2} \frac{L_{tank}^2 \omega^4}{V_{sw}^2} \sum_n \left(\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{rms,n}^2\right) \qquad (1)$$

where f_{off} is the offset frequency from the carrier. Γ_{rms}^2 is the *rms* value of the *impulse sensitivity function* (ISF) [1] and is 1/2 for an ideal sinusoidal waveform. It can be evaluated more accurately from simulation as discussed in the subsequent sections. Each $\overline{i_n^2}/\Delta f$ in the sum represents drain current noise, gate noise, inductor noise, and varactor noise. The equivalent differential noise due to the drain current noise and the gate noise of the MOS transistors are given by $2kT\gamma(g_{d0,n} + g_{d0,p})$ and $(2kT\delta\omega^2/5g_{d0})(C_{gsn}^2 + C_{gsp}^2)$ [1], respectively, where $\gamma \sim 2.5$ for short channel devices and $\delta \sim 2\gamma \sim 5$. g_{d0} is the drain-source conductance at zero V_{DS} and given by $I/(LE_{sat})$ in deep short channel regime [1]. The inductor noise and varactor noise are given by $2 \cdot 4kTg_L$ and $2 \cdot 4kTg_{v,max}$, respectively, where $g_{v,max}$ imposes the worst-case condition.

3.3. Linear Programming

In this section, the design optimization process for the 2.4GHz oscillator through linear programming will be demonstrated. The constraints can be graphically represented as in Figures 8 to 11 in the xy space for various magnitude of bias current, where w is W_n in μm and c is $C_{v,max}$ in pF. On the right side of the start-up line, loop gain is over 3 and start-up is easy. A tuning range of at least 15% with a center frequency of 2.4GHz is achieved if a design point stays below the tr1 line and above the tr2 line, where the tr1 and tr2 line define the maximum and minimum frequency of the tuning. Below the voltage swing line, the voltage swing is over 2V. The shadowed regions satisfy all the constraints. The broken lines with one dash and three consecutive dots in Fig. 9 to 11 represent $2.5V$ voltage swing lines. The oscillation occurs in

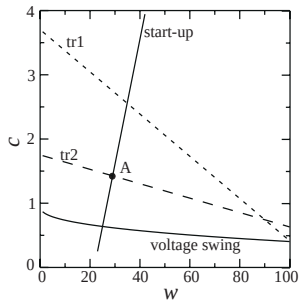

Figure 8: 2.5mA constraint

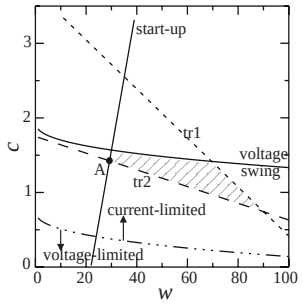

Figure 9: 3mA constraint

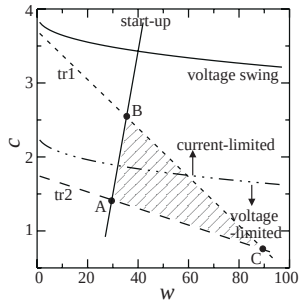

Figure 10: 4mA constraint

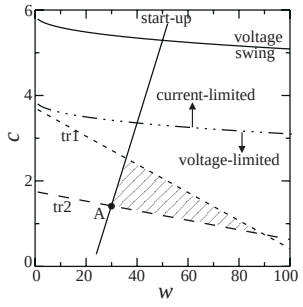

Figure 11: 5mA constraint

the voltage-limited regime rather than in the current-limited regime below these curves and the magnitude of the voltage swing is around 2.5V [1].

The tuning range constraint remains the same independent of the bias current. Also, the start-up constraint shows weak dependence on the bias current as the transconductance of transistors in short channel regime is hardly dependent on the bias current. However, the voltage swing constraint strongly depends on the bias current. For $I = 2.5mA$, all the constraints imposed cannot be met at the same time. As the bias current increases, shadowed areas are generated and for $I = 4mA$ and $I = 5mA$, the voltage swing constraint becomes the necessary condition for the first tuning range constraint.

Using the general expressions for device noise and a Γ_{rms} of 1/2, phase noise at 600kHz offset from a 2.4GHz carrier is given by

$$\mathcal{L}(w,c;i) = \frac{2.22\times10^{-13}(c + 1.58\times10^{-3}w^2 i^{-1} + 4.06i + 4.02)}{V_{sw}^2(w,c;i)} \quad (2)$$

where i represents current in mA and serves as another parameter. For $I = 5mA$, the oscillation occurs in the deep voltage-limited regime as seen in Fig. 11. Henceforth, $\mathcal{L}(w,c;i)$ becomes minimum where the numerator of (2) which is defined as $f(w,c;i)$ becomes minimum. Since the slope of tr2 line is 0.011 and is smaller than $\frac{d}{dw}(\frac{1.58\times10^{-3}}{i}w^2)|_{w=30} = \frac{9.48\times10^{-2}}{i}$ for $I \leq 8.6mA$, we obtain the minimum phase noise at point $\mathbf{A}(30\mu m, 1.42pF)$ in Fig. 11. The calculated phase noise at this point is $-120dBc/Hz$ at 600kHz offset from a 2.4GHz carrier.

In Fig. 10 ($I = 4mA$), some of the shadowed region is in the voltage-limited regime while the rest of the shadowed region is in the current-limited regime. The point **A** which minimizes $f(w,c;i)$ maximizes $V_{sw}(w,c;i)$ as it is in the voltage-limited regime, and accordingly the phase noise is minimized at **A** again. The calculated phase noise is $-121dBc/Hz$ at 600kHz offset from a 2.4GHz carrier. We are designing the oscillator with $4mA$ of tail current and thus, $W_n = 30\mu m$ and $C_{v,max} = 1.42pF$ are the optimum design variables we used for the transistor and varactor. At this operation point, the noise contributions of drain current noise, gate noise, inductor noise, and varactor noise are 74%, 2%, 18%, and 6%, respectively.

As can be seen, once the oscillator operates in the voltage-limited regime, the minimization of the phase noise becomes easier, by reducing the complicated denominator in (2) to a constant value. While the phase noise decreases as current increases until the oscillation reaches the voltage-limited regime, once the oscillator enters the voltage-limited regime, the phase noise begins increasing as the current is further increased, as seen from (2). The critical current value is obtained by having point **A** at the verge of the voltage limited regime, *i.e.*, on the regime-divider line, and thus, the lowest phase noise is obtained with the highest power efficiency. In this design, $I_{critcal}$ is $3.7mA$ from a numerical method. The phase noise calculated at this current is -121dBc/Hz at 600kHz offset from 2.4GHz.

The phase noise values calculated here are approximate since the value for E_{sat} is estimated from device data and Γ_{rms} is approximated with 1/2. Also, all the variables used are derived from small signal analysis while some constraints such as voltage swing require large signal analysis. Finally, the symmetric inductor model used for the linear programming is rather approximate as mentioned earlier. A more accurate phase noise prediction will be obtained in the next section.

4. SIMULATION

Simulation is performed with a tail current of 4mA using the inductor model in Fig. 4. The node names mentioned in this section are with reference to Fig. 1.

As the oscillator is tuned between minimum and maximum oscillation frequency, its voltage swing changes from 1.75V to 1.94V and therefore the oscillation occurs in the current-limited regime. This discrepancy can be attributed to the different inductor models in linear programming and simulation and approximate small signal model using estimated E_{sat} in linear programming.

Simulations to estimate the phase noise are performed at $2.22GHz$. The *impulse sensitivity functions* (ISF) of various noise sources are obtained by performing the charge injection simulation [1]. The simulated ISF of various noise sources is depicted in Fig. 12. The Γ_{rms} values are 0.50 and 0.52 for the NMOS and PMOS transistors, respectively.

The time-varying cyclostationary effect of the drain current noise due to the gate-source voltage variation can be taken into account by expressing the equivalent differential noise due to the drain current noise in the following form:

$$\frac{\overline{i_{M,drain}^2}}{\Delta f} = 4kTg_{d0,eq,n}(\frac{g_{d0,n}}{g_{d0,eq,n}}) + 4kTg_{d0,eq,p}(\frac{g_{d0,p}}{g_{d0,eq,p}}) \quad (3)$$

where the subscript eq corresponds to the unstable equilibrium when $v(1) = v(2) = 1.15V$ and $g_{d0,eq}$ is the drain-source conductance at zero V_{DS} at the equilibrium. Here, $g_{d0}/g_{d0,eq}$ is the square of the *noise modulating function* (NMF) [1]. The simulated NMF and the effective ISF which is the product of the ISF and NMF for the drain current noise are depicted in Fig. 13 and 14, respectively. The $\Gamma_{eff,rms}$ is 0.45 for NMOS and 0.52 for PMOS and hence the drain current noise including the effect of Γ_{rms} is $6.90\times10^{-23}A^2/Hz$ where we used

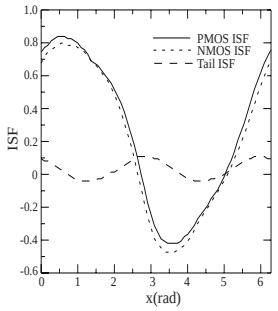

Figure 12: ISF

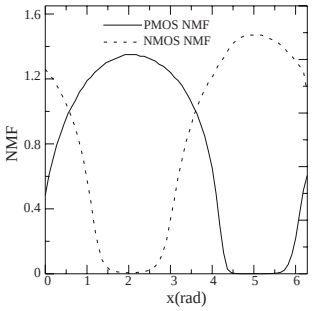

Figure 13: NMF

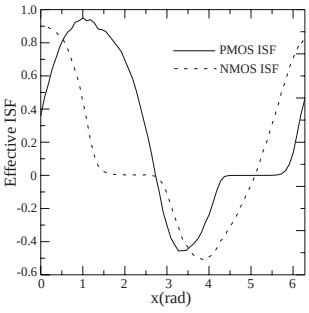

Figure 14: Effective ISF

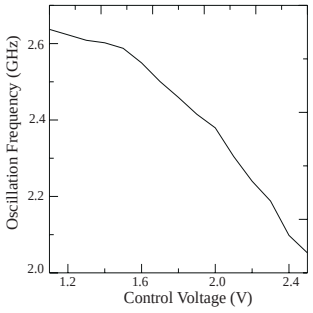

Figure 15: Frequency tuning

$\Gamma_{eff,rms}$ instead of Γ_{rms} in (1). The cyclostationary channel noise of the tail current transistor can be similarly obtained [1] and its value is $3.73 \times 10^{-24} A^2/Hz$. Since the transistor gate noise only has a small contribution to the total phase noise as shown in the previous section, its time-varying effect can be neglected.

The total simulated phase noise is -120dBc/Hz at 600kHz offset from a 2.22GHz carrier. Drain current noise, gate noise, inductor noise, varactor noise, and tail noise contribute 69%, 1%, 18%, 7% and 5% of phase noise in the circuit, respectively. The simulation result shows only 1dB difference from the prediction made in the previous section. The $1/f$ noise reduction factors are 0.18 and 0.25 for NMOS and PMOS transistors, respectively [1].

5. EXPERIMENTAL RESULTS

Table 1 summarizes performance of the VCO, which was implemented in three-metal, $0.35\mu m$ Conexant's BiCMOS technology. A tuning range of 26% is achieved as shown in Fig. 15. Phase noise is measured using an HP8563 spectrum analyzer with phase noise measurement utility. The measured phase noise at 2.2GHz is about 3dB higher than the simulated phase noise. This 3dB difference can be attributed to the uncertain channel noise constant γ, degradation of voltage swing caused by the parasitic resistors in metal layers and high sensitivity of the oscillation frequency to extrinsic supply and control line noise due to the high VCO gain at

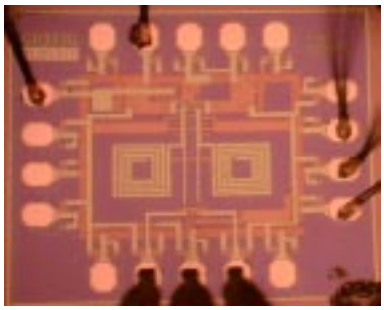

Figure 16: Chip photograph

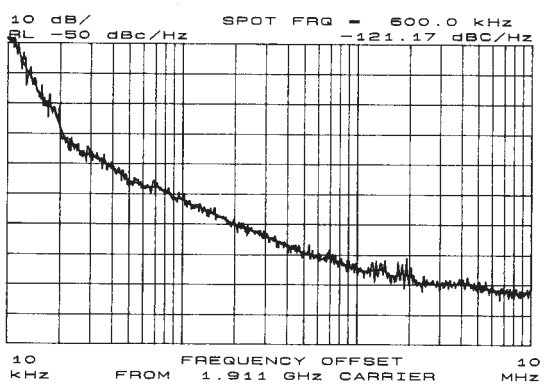

Figure 17: Phase noise vs. f_{off} at 1.91GHz

this frequency. Fig. 17 shows a plot of phase noise vs. offset from the 1.9GHz carrier.

Supply voltage	2.5V
Current (core)	4mA
Center frequency	2.33GHz
Tuning range	26 %
Output power	0dBm
Phase noise ($f_c = 1.91GHz$, @$600kHz$)	-121dBc/Hz
Phase noise ($f_c = 2.03GHz$, @$600kHz$)	-117dBc/Hz
Phase noise ($f_c = 2.63GHz$, @$600kHz$)	-115dBc/Hz

Table 1 : VCO performance summary

6. CONCLUSION

Phase noise of a voltage controlled oscillator was minimized via linear programming under constraints on the minimum voltage swing, tuning range, and loop gain. The linear programming technique provides design insight via a graphical representation of design parameters. A tuning range of 26% was achieved with the MOSCAP tuning. The measured phase noise was -121dBc/Hz, -117dBc/Hz and -115dBc/Hz at 600kHz offset from 1.91GHz, 2.03GHz and 2.60GHz carriers, respectively. The designed VCO dissipates only 4mA from a 2.5V supply voltage.

7. ACKNOWLEDGMENT

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