21.2 A Circular Standing Wave Oscillator

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This paper introduces a new class of oscillators that generate sinusoidal signals by formation of a circular standing wave on a ring (closed-loop) transmission line (t-line). A basic form of the circular standing wave oscillator (CSWO), schematically illustrated at the top left of Fig. 21.2.1, consists of a ring t-line and two pairs of cross-coupled inverters located at two opposite ports on the ring. The ring t-line provides a frequency selection mechanism while the cross-coupled inverters compensate loss in the ring.

Multi-mode standing waves are formed on the ring to meet the periodic boundary condition that requires the voltage, $V(\phi)$, on the ring at any angle, ϕ, to be equal to $V(\phi+2\pi)$. For any given standing wave mode, the ring's circumference, l, is an integer multiple, n, of the wavelength, λ, of the mode. The top middle and right of Fig. 21.2.1 conceptually depict the fundamental (n = 1) and the second (n = 2) modes, respectively, each with loud and quiet ports. The absolute positions of the loud/quiet ports are determined by the position of the energy injection that creates the resonance. In the basic form of the CSWO of Fig. 21.2.1 (top left), ports T1-T2 and B1-B2 where energy is injected by the cross-coupled inverters remain always loud for all modes. Ports L1-L2 and R1-R2 are quiet for odd modes and loud for even modes.

The CSWO implementation reported in this paper, schematically shown at the bottom left of Fig. 21.2.1, takes a step further and incorporates an even-mode suppression technique as well. By connecting T1 to B2, and T2 to B1 (broken lines), we ensure port T1-T2 and port B1-B2 remain always in opposite phase, which is possible only for odd modes. Therefore these two connections suppress even modes, and ports L1-L2 and R1-R2 remain always quiet. The T1-B2 and T2-B1 interconnects should introduce delay negligible compared to the delay in the ring. This can be achieved by bending the ring so that ports T1-T2 and B1-B2 are physically positioned proximate each other in the layout, as depicted at the bottom right of Fig. 21.2.1. The major rationale for the even mode suppression is to concentrate more energy in the odd modes (practically, the fundamental mode), in order to improve the voltage swing and the phase noise performance at the fundamental frequency for a given power consumption. The even-mode suppression also lowers the harmonic distortion.

It is necessary, at this point, to compare the CSWO to relevant recent works in oscillators utilizing wave phenomena [1] - [5] (Fig. 21.2.2). Traveling wave oscillators (TWO) [1] [2] are constructed by connecting the output of a traveling wave amplifier back to its input. Two disadvantages of the TWO, the waste of the reverse wave energy and noise generation by the termination resistors [6], are overcome by cross-coupling the output and input lines, eliminating the termination resistors. This rotary traveling wave oscillator (RTWO) in [3] also replaces the one-directional amplifiers in the TWO with cross-coupled inverters, allowing use of a differential t-line. Works in [4] [5] report standing wave oscillators (SWO) generating standing waves via reflective boundary conditions caused by impedance mismatch. Our CSWO deviates both topologically and operationally from these works. Important distinctions are its use of the periodic boundary condition and the even mode suppression technique.

As a prototype, we implemented a 10GHz monolithic CSWO using a SiGe bipolar technology with f_T of about 50GHz and three Al metal layers. The differential ring t-line is realized in the form of a closed-loop coplanar stripline (CPS) using a thick (3μm) top metal layer. Figure 21.2.3 shows the final layout of the CPS together with the schematically drawn cross-coupled inverters and even-mode suppression interconnects (two curved lines in Fig. 21.2.3). The ring CPS is bent to bring the two loud ports close in order to minimize delay in the even-mode suppression connections. To reduce the chip area, the two quiet ports were put close to each other as well, resulting in the clover shape CPS. The CPS was modeled using Sonnet EM simulation. Two-port s-parameters for the $\lambda/4$ section of the CPS (Fig. 21.2.3) generated in the EM simulation were converted to multi-section differential L-R-C-G parameters to be used in time-domain circuit simulations. The $\lambda/4$ section was designed in such a way to keep the characteristic impedance uniform, S_{21} phase 90° at 10GHz, and loss minimal. Since the EM simulation predicted insignificant coupling between the adjacent $\lambda/4$ sections, the simple 2-port modeling based on the $\lambda/4$ section was used. Along the CPS, the metal width varies between 30μm and 60μm, and the metal separation varies from 7μm to 14μm. The total lengths of the outer and the inner metals of the CPS are around 4.3mm. The two slightly different lengths of the outer and the inner metals do not result in two different fundamental frequencies, because the electrons in the two metals have proportionally different linear speeds, resulting in the same angular velocity. The characteristic impedance of the CPS is about 55 Ω and the quality factor estimated from the simulated s-parameters is about 8. A die photo of the CSWO is shown in Fig. 21.2.4; the chip area is 2×2.1 mm².

In this special prototype of Fig. 21.2.3, due to the npn-only cross-coupling, the V_{dd} for the active devices is to be provided at only one of the two quiet ports. This mode of power supply adds a redundant reflective boundary condition on top of the periodic boundary condition. The even-mode suppression connections are still necessary even with the V_{dd} applied at the quiet port, since without the connections the oscillator can conditionally excite an $l = \lambda/2$ mode (half the design frequency) in which the maximally loud port is not where the inverters are connected, but port L1-L2 of Fig. 21.2.1. In general, depending on the gain cell configuration, V_{dd} can be directly connected to some node in the gain cell (e.g. complementary npn-pnp cross-coupling), or connected at the quiet port.

Figure 21.2.5 shows the measurement setup for the single-ended output. While the loud ports are the only important ports in practice, we probe the quiet ports as well to demonstrate the formation of the circular standing wave and the suppression of the even modes. The oscillator core is interfaced with an Agilent E4448A spectrum analyzer via on-chip open-collector npn buffers and off-chip bias-tees. Six chip samples were measured. Measured oscillation frequencies vary from 9.7GHz to 10.3GHz chip-to-chip, proving the reasonable accuracy of our CPS modeling. The output power at the loud port varies from -18dBm to -15dBm chip-to-chip, where these readouts from the E4448A should be adjusted for the measured insertion loss of 5dB from the RF probes to the spectrum analyzer.

Figure 21.2.6 shows output spectra at the loud and quiet port measured after the npn buffers. At the fundamental oscillation frequency (~ 10GHz), the quiet port has about 38dB less power than the loud port, confirming the formation of the circular standing wave at the fundamental mode. At the frequency twice the fundamental oscillation frequency (~ 20GHz), the quiet port has a very low output power (~ -70dBm) verifying successful even-mode suppression, since the 2nd standing wave mode would maximally vibrate at the quiet port were it not for the even-mode suppression connections. The strong nonlinearity of the npn buffer contributes the 2nd harmonic in the single-ended measurement at the loud port through distortion of the strong fundamental mode at the same loud port.

Figure 21.2.7 shows phase noise versus offset frequency measured using a phase noise personality of the E4448A. The phase noise at 1MHz offset is -110dBc/Hz with a core current from the 1.5V supply of only 1.95mA (hence a low power consumption of ~ 3mW), and an output power of about -15dBm.

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[5] F. O'Mahony et al., "10GHz Clock Distribution Using Coupled Standing-Wave Oscillators," *ISSCC Dig. Tech. Papers*, pp. 428-429, Feb. 2003.
[6] C. J. White et al., "Phase Noise in Distributed Oscillators," *Electronics Letters*, vol. 38, no. 23, pp 1453-1454, Nov. 2002.

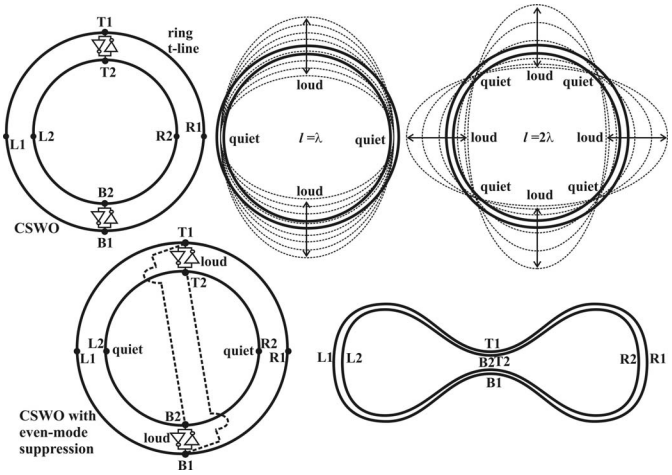


Figure 21.2.1: Circular standing wave oscillator (CSWO).

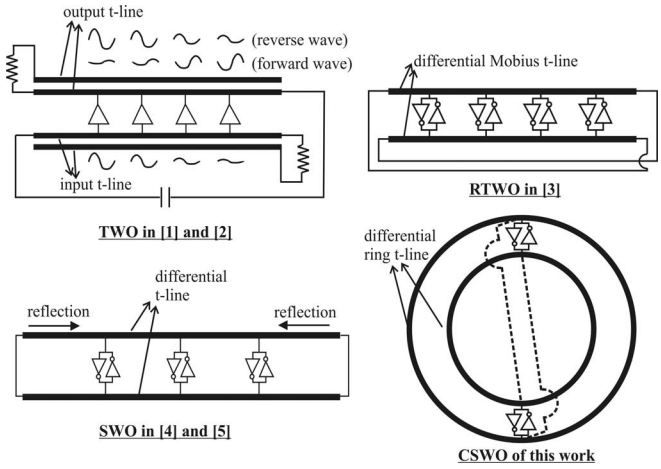


Figure 21.2.2: Comparison with relevant recent works on oscillators utilizing wave phenomena.

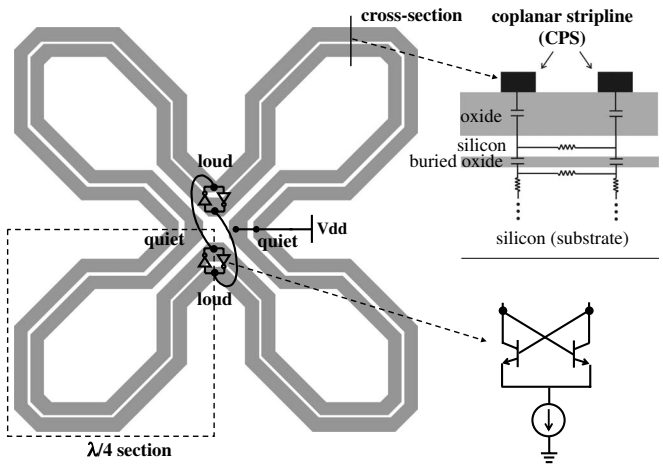


Figure 21.2.3: Implementation of the CSWO.

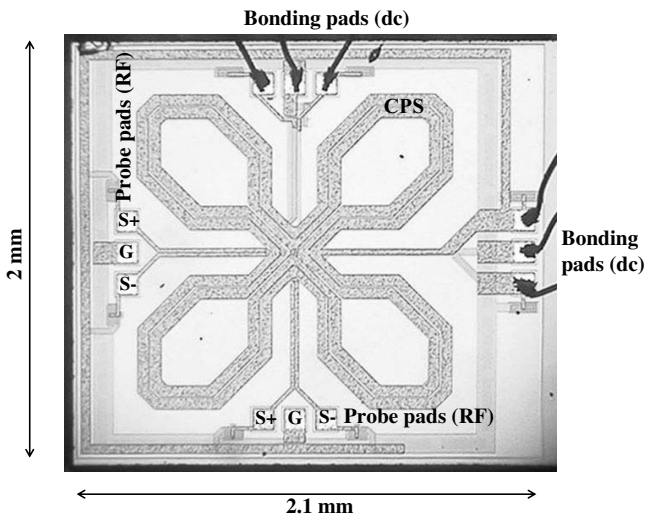


Figure 21.2.4: Chip photo.

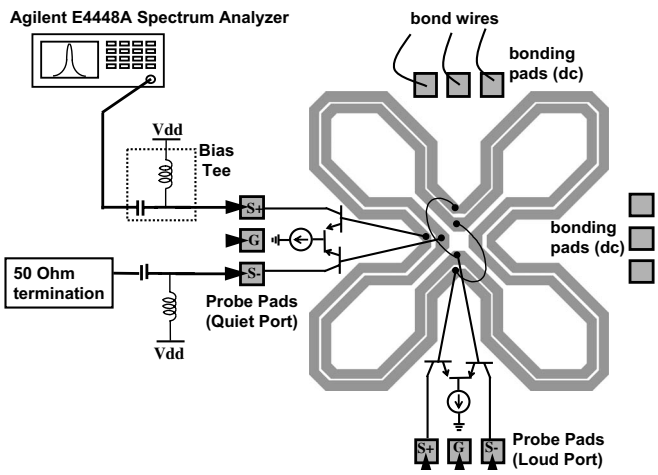
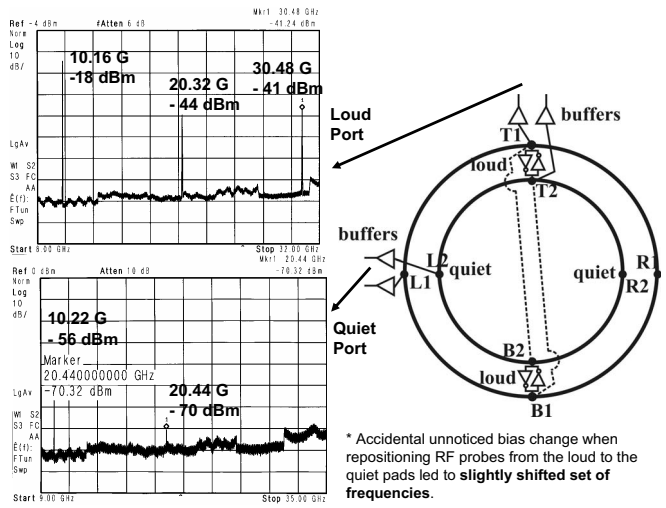


Figure 21.2.5: Measurement setup.



* Accidental unnoticed bias change when repositioning RF probes from the loud to the quiet pads led to **slightly shifted set of frequencies**.

Figure 21.2.6: Spectrums of the 10GHz CSWO.

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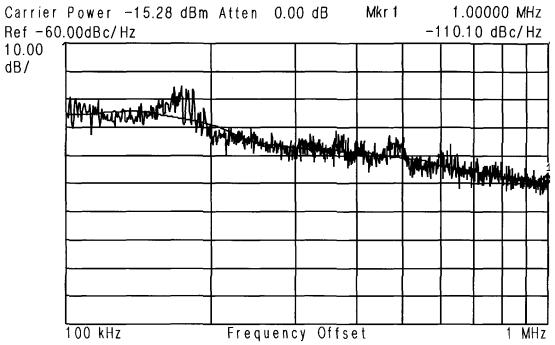

- **Supply voltage: 1.5V**
- **Current (oscillator core): 1.95mA**

} **Power dissipation ~ 3mW**

- **Center frequency: 10.17 GHz**
- **Output power (single-ended @ loud port): -15.3 dBm**
- **Phase noise @ 1MHz offset: -110 dBc/Hz**

Figure 21.2.7: Measured phase noise and performance summary.