STANDING WAVE OSCILLATORS UTILIZING WAVE-ADAPTIVE TAPERED TRANSMISSION LINES

William Andress and Donhee Ham

Harvard University, Cambridge, MA 02138, USA

ABSTRACT

This paper introduces a novel standing wave oscillator (SWO) utilizing a tapered transmission line adapted to the position-dependent amplitudes of standing waves. The tapered line fully exploits the core property of standing waves to enhance Q and lower phase noise, demonstrating the benefits of wave-based oscillators. Measurements confirm the advantages of the proposed technique. The phase noise of a fully-integrated MOS SWO with the tapered line is about 8 dB superior to that of a uniform-line SWO over a wide range of offset frequencies, where the oscillation frequencies are around 15 GHz.

Keywords: oscillators, standing wave oscillators, transmission lines, tapered transmission lines, quality factors, phase noise, radio frequency, CMOS integrated circuits.

1. INTRODUCTION

Recently there have emerged oscillators relying on wave phenomena as an alternative to LC oscillators. Wave-based oscillators are categorized into traveling wave oscillators [1] - [3] and standing wave oscillators [4] - [6]. While the benefits of the wave-based oscillators in certain design criteria (*e.g.*, high-frequency oscillation [1] [2], low-jitter low-skew clock distribution [5]) are evident, it has not been clear whether the wave-based oscillators could be more advantageous than LC oscillators in achieving a superior phase noise. This paper addresses the issue and presents a case where exploitation of wave behaviors proves beneficial in enhancing Q and lowering phase noise.

Standing waves have the unique property of position-dependent voltage-current amplitudes. This paper demonstrates that transmission lines that host standing waves readily lend themselves to a position-dependent structuring. One can physically *taper* a transmission line adapted to the standing wave amplitude variations to reduce loss in the line, leading to Q improvement and phase noise reduction in standing wave oscillators (SWO). In the prototype tapered-line MOS SWO presented in this paper, the simulated effective Q of the tapered line hosting standing waves is about 59, a considerable improvement over the Q of 39 achieved before tapering. Phase noise measurements attest to the validity of the proposed technique.

Section 2 introduces a $\lambda/4$ SWO, which we will use as a vehicle for demonstration of the concept. Sections 3 and 4 discuss concepts and design of the tapered-line SWO, respectively. Measurements confirming the benefits of the proposed technique are presented in Sec. 5.

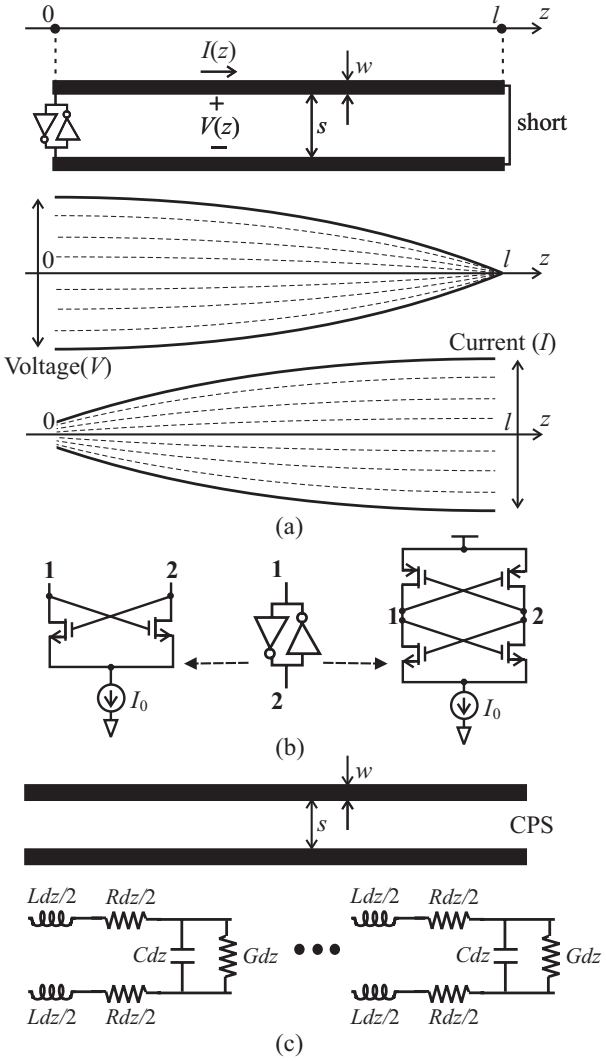

Figure 1: (a) $\lambda/4$ SWO and standing waveforms at the fundamental mode. (b) MOSFET implementations of the cross-coupled inverters. (c) Coplanar stripline and differential $LRCG$ model.

2. $\lambda/4$ STANDING WAVE OSCILLATOR

A quarter-wavelength ($\lambda/4$) SWO of Fig. 1(a) will be used as a vehicle to demonstrate the validity of the proposed technique. In the SWO a differential transmission line is connected to a pair of cross-coupled inverters at one end and is shorted at the other end. The cross-coupled inverters may be realized using cross-coupled NMOS or CMOS transistors as shown in Fig. 1(b). The differential transmission line is implemented in the form of an on-chip coplanar stripline (CPS) in silicon as shown in Fig. 1(c).

In the SWO of Fig. 1(a) energy injected by the cross-coupled inverters propagates in forward waves along the

line toward the short, where the energy is reflected into reverse waves. In steady state, the forward and reverse waves superpose to form standing waves. While boundary conditions allow standing wave modes at $l = \lambda/4 \times n$ ($n = 1, 3, 5, ...$), we will only consider the fundamental mode ($l = \lambda/4$) since higher modes are of relative insignificance due to substantial high-frequency loss.

In the fundamental mode, voltage amplitude, $V(z)$, and current amplitude, $I(z)$, exhibit monotonic variations with z as depicted in Fig. 1(a). The voltage minimum (zero) and current maximum occur at the short end ($z = l$) while the voltage maximum and current minimum occur at $z = 0$. Due to transistor loading, the amplitude of this current minimum at $z = 0$ is slightly larger than zero, as l is slightly smaller than $\lambda/4$.[1] This amplitude variation in standing waves proves very useful in lowering SWO phase noise, as shown in the following section.

3. LINE TAPERING IN SWO – CONCEPTS

Figure 1(c) shows the familiar differential $LRCG$ model for an on-chip CPS where L, C, R, and G are inductance, capacitance, series resistance, and shunt conductance per unit length, respectively. R mainly accounts for loss within metals due to skin and proximity effects while G reflects loss outside metals (*e.g.*, substrate loss). R couples to current waves as G couples to voltage waves to introduce respective series and shunt losses. Smaller R corresponds to less series loss; smaller G corresponds to less shunt loss.

R and G of the CPS can be modified by varying the metal width, w, and the separation, s, of the CPS, where w and s are with reference to Fig. 1(c). Increasing s or w decreases R due to reduced proximity/skin effects but increases G due to increased interaction between EM fields and lossy media outside the metals (substrate, underlying metals, etc.)[2]. This tradeoff between the series loss, R, and the shunt loss, G, imposes a major constraint in loss minimization when the CPS carries a traveling wave.

When the CPS hosts a standing wave, the R-G tradeoff can be elegantly circumvented to minimize loss, thanks to the position-dependent standing wave amplitudes. Since the $\lambda/4$ CPS of Fig. 1(a) has large voltage amplitude and negligible current amplitude near $z = 0$ and vice versa near $z = l$, the majority of loss is through shunt conductance G toward $z = 0$ and through series resistance R toward $z = l$. Therefore, G may be minimized to reduce loss near $z = 0$ while the unavoidable increase in R is not detrimental because of the negligible current amplitude in this vicinity. Similarly toward $z = l$, R may be minimized to reduce loss while the inevitable increase in G is not harmful due to the locally negligible voltage.

[1]The effect of loading upon the wavelength makes frequency tuning feasible. Varactors may be placed adjacent to the gain cell to vary the degree of loading [7].

[2]EM simulation results presented in Sec. 4 elucidate these tendencies.

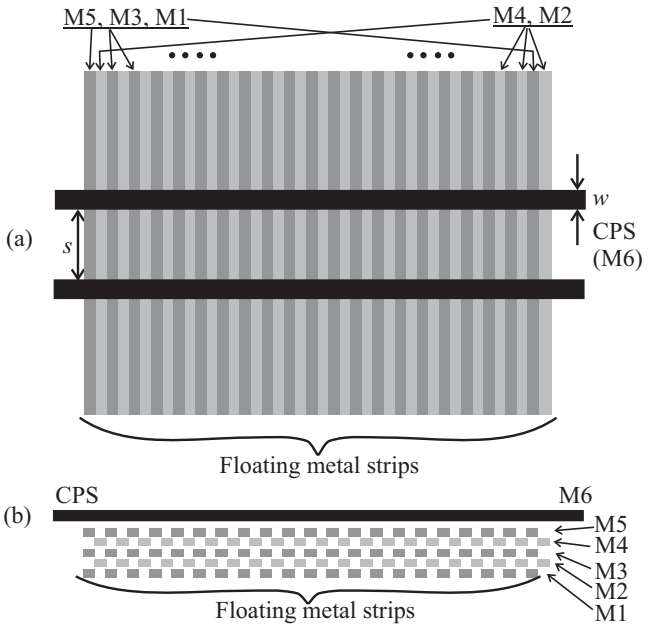

Figure 2: CPS over floating metal strips (a) top view (b) side view

This continuous variation of R and G along z to minimize loss yields a *tapered* transmission line. The quantitative degree of loss reduction owing to the tapering depends on the mathematical nature of the R-G tradeoff, which varies from process to process. The following section will quantitatively present the loss reduction using a specific design.

The CPS tapering should be performed with attention to holding the characteristic impedance constant throughout the line to prevent partial reflections. The design of a tapered CPS with constant impedance is now presented.

4. LINE TAPERING IN SWO – DESIGN

The design of a tapered CPS with a uniform characteristic impedance is greatly facilitated using a comprehensive set of data acquired through Sonnet EM simulations for a wide range of w and s values. The layered metal structure[3] used in simulation is depicted in Fig. 2, where the floating metal strips serve to retard the wave [8], which decreases the necessary CPS length and overall layout area to support a given frequency. The floating metal strips significantly reduce the substrate effect as well [7]. The SWOs employing the simulated structures were designed for 15 GHz oscillation.

The impedance and loss contours in w-s space shown in Fig. 3(a) capture the essential results of the EM simulations. The R and G contours *roughly* coincide. The contours reveal a method for varying R and G without altering the characteristic impedance, Z_0. Increasing either w or s results in a decreased R and increased G due to the R-G tradeoff mentioned earlier. However, Z_0 increases with increasing s but decreases with increasing w. Therefore to achieve low G near $z = 0$ and low R at $z = l$ to minimize loss without affecting Z_0, one can simulta-

[3]in a 0.18μm CMOS technology with a thick top-metal layer.

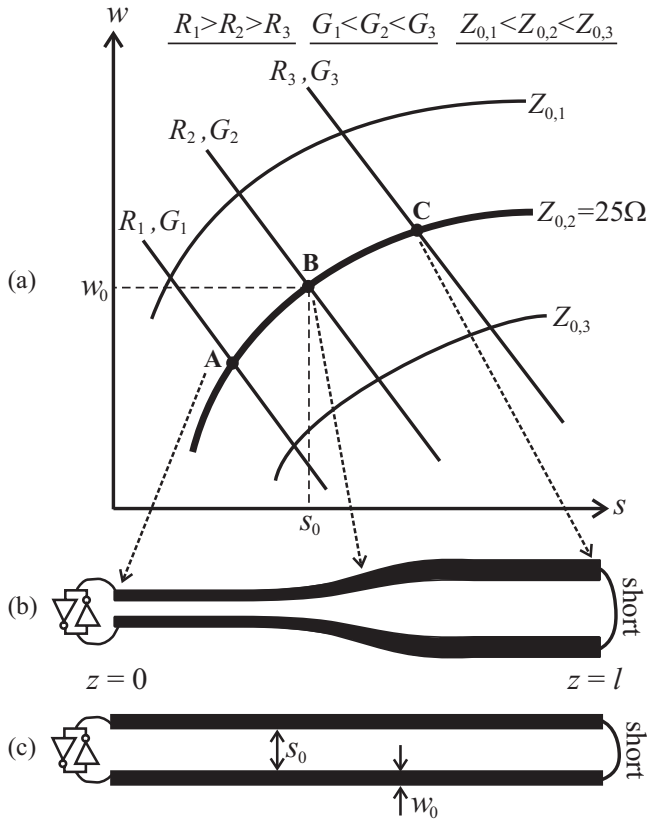

Figure 3: (a) Impedance and loss contours based on EM simulation data. The R and G contours *roughly* coincide. (b) $\lambda/4$ SWO using a tapered CPS with $Z_0 = 25\Omega$. (c) $\lambda/4$ SWO using an optimum-loss uniform CPS with $Z_0 = 25\Omega$.

#	w (μm)	s (μm)	R ($m\Omega$/deg)	G (μS/deg)	Points in Fig. 3(a)
1	75	20	3.10	.808	**A**
2	80	30	2.43	.999	
3	85	50	1.54	1.99	**B**
4	90	100	.814	4.74	
5	90	120	.491	6.32	**C**

Table 1: Simulated loss parameters (per degree of phase shift) for the implemented 25Ω tapered CPS at different points.

neously widen and move apart the CPS metals towards $z = l$ following a Z_0 contour as shown in Figs. 3(a) and (b). We arbitrarily chose $Z_0 = 25\Omega$. Parameters describing the 25Ω tapered CPS at various positions are given in Table 1, where row 1 provides those of point **A** in Fig. 3(a) (employed at voltage maximum, $z = 0$) and row 5 provides those of point **C** in Fig. 3(a) (employed at current maximum, $z = l$). Between the two boundaries the CPS assumes a continuous range of values between points **A** and **C** along the $Z_0 = 25\Omega$ contour, with intermediate w and s values interpolated from the those shown in Table 1. Beyond this range loss characteristics do not favor tapering [7]. The optimal apportionment of the various 25Ω configurations in the tapered CPS was determined through a mathematical procedure [7] too lengthy to be described here, and adjusted based on schematic simulation to account for transistor loading.

For comparison, a 25Ω uniform CPS, as in Fig. 3(c), was designed as well. Rather than assuming a range of w and s values, the uniform-CPS parameters are those of point **B** for its entire length. This point was chosen because the corresponding loss values, R_2 and G_2, are those that minimize total dissipation of the standing wave in the uniform line.

Calculation using the design parameters shows that the loss of the tapered CPS is 0.67 that of the optimum uniform CPS for a given standing wave energy stored. This translates to a 50% improvement in Q. The optimum uniform CPS has a simulated Q of 39 at 15 GHz[4], but the tapered CPS hosting the standing wave has an even higher effective Q of $39 \times 1.5 \approx 59$, a considerable number for an on-chip resonator implemented in a standard silicon technology. The loss reduction by a factor of 0.67 also corresponds to signal power P_s (at the oscillator *core*) enhancement by a factor of approximately 1.5 for a given *dc* power consumption, as verified in circuit simulations. The familiar Leeson's formula [9]

$$\mathcal{L}\{\Delta\omega\} = F\frac{kT}{2P_s}(\frac{\omega}{Q\Delta\omega})^2$$

then predicts that phase noise improves by an approximate factor of $1.5^3 \approx 5.3$dB. This calculation serves to convey a rough idea on the phase noise improvement; the following section shows that the measured phase noise improvement is more than 5.3dB.

Figure 4 shows the die photo for the implemented uniform- and tapered-CPS SWOs. They have exactly the same design except the CPS structures, and were implemented adjacently on the same die. Each circuit occupies an area of 1.2×1.2 mm^2; both CPS structures span about 420μm. We used NMOS-only gain elements (Fig. 1(b)) and the V_{dd} was provided at the shorted end.

One perceivable problem with the $\lambda/4$ SWO, especially that with a tapered CPS, involves the design of the electrical short. The greater line separation around $z = l$ in the tapered CPS requires a proportionally long "short," increasing series resistance where it is most detrimental and undermining the benefits of tapering. To alleviate this problem, all underlying metal layers were added to the short (in both the uniform- and tapered-CPS circuits) to substantially reduce the series resistance in the short.

5. EXPERIMENTAL VERIFICATIONS

The voltage outputs of the SWO at $z = 0$ were interfaced with an Agilent E4448A spectrum analyzer via on-chip open-drain NMOS buffers, RF probes and cables, and bias-Tees. The spectrum analyzer has a built-in phase noise measurement system. A tapered- and a uniform-CPS SWO on the same die were measured under the same bias condition to determine the phase noise improvement due to tapering. The measurement results are summarized in Table 2. The oscillation frequency is 14.2 GHz for the tapered-CPS SWO and 15.6 GHz for the uniform-CPS SWO, slightly deviating from the design frequency,

[4]This high Q is due to the floating metal strips [7].

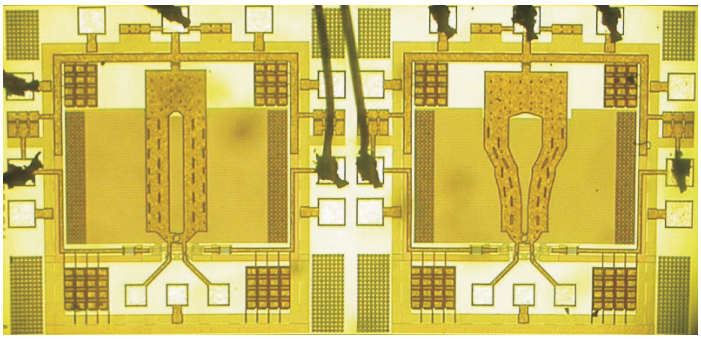

Figure 4: (Left) MOS SWO with uniform CPS (Right) MOS SWO with tapered CPS.

SWO type	Tapered CPS	Uniform CPS
f_0 (GHz)	14.2	15.6
Vdd (V)	1.8	1.8
I_0 (mA)	2.6	2.6
P_{out} (dBm)	-12	-15
$\mathcal{L}\{1\text{MHz}\}$ (dBc/Hz)	-110	-102

Table 2: Measurement results from the SWOs under the same bias condition. P_{out} is the power transfer to a 50Ω load driven by an on-chip open-drain buffer.

15 GHz. The noticeably low *dc* power consumptions are indirect evidence of the high Q of the lines.

The tapered-CPS SWO has a reduced phase noise as compared to the uniform-CPS SWO, *e.g.*, 8 dB reduction at 1 MHz offset. The unexpected frequency discrepancy between the two circuits could be partially responsible for the improvement, but EM simulations combined with Leeson's formula [9] show that this accounts for no more than 1 dB difference. Identically sized transistors were used in each design for fair comparison. But the significantly reduced loss in the tapered-CPS allows one to shrink the transistors in the tapered-CPS SWO, which would further benefit phase noise performance.

Figure 5 shows measured phase noise vs. offset frequency for the uniform-CPS SWO and the tapered-CPS SWO over 3 decades of offset frequencies. The phase noise improvement due to the tapering is at least 5 dB between 10 kHz and 1 MHz where the $1/f^3$ behavior is pronounced. At greater offset frequencies where the white noise effect dominates and $1/f^2$ behavior is apparent, the improvement is 8 to 10 dB.

Due to the loss difference between the uniform- and tapered-CPS SWO, the identical bias condition may place the two circuits in different regions of operation. In order not to allow any advantage for the tapered-CPS SWO, the uniform-CPS SWO was measured under various other bias conditions, but the overall phase noise reduction of at least 8dB persisted. Three more chip samples (each contains a tapered and a uniform circuit) were measured, and the essential measurement results presented above occurred consistently.

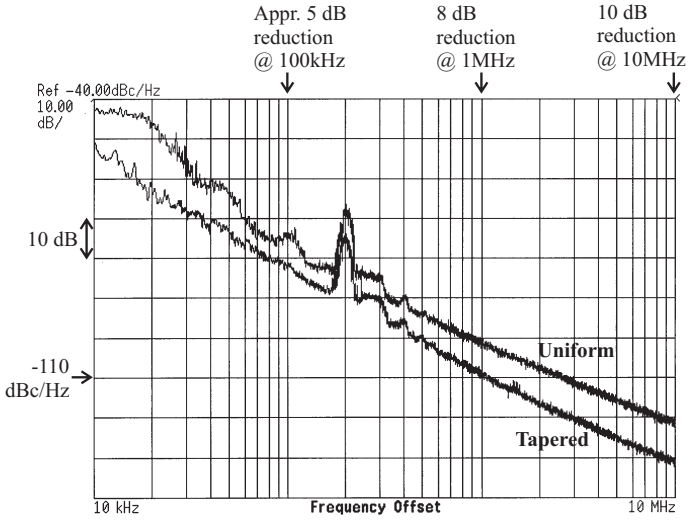

Figure 5: P.N. vs. f_{off} for the tapered- and uniform-CPS SWOs.

6. CONCLUSION

We showed that a transmission line hosting standing waves can be shaped according to the position-dependent standing wave amplitudes to improve Q and phase noise of standing wave oscillators, explicitly demonstrating the advantages of wave-based oscillators. We also presented the methodology to design the tapered line with a constant characteristic impedance. The on-chip tapered CPS presented has a Q of 59, enhanced by almost 50% as compared to the optimum uniform CPS. This improvement was reflected in a remarkable phase noise reduction of 8 to 10 dB in the tapered-line SWO in comparison to the uniform-line SWO. Although this demonstration involved a $\lambda/4$ SWO, it may be applied to *any* form of SWOs.

7. ACKNOWLEDGMENT

The authors thank Christopher White of Caltech and Yong Liu and David Ricketts of Harvard University for their valuable suggestions and Sonnet for their field solver donation. This work was supported by an IBM gift.

8. REFERENCES

[1] B. Kleveland *et al.*, "Monolithic CMOS distributed amp. and osc.," *IEEE ISSCC Dig. Tech. Papers*, pp. 70-71, Feb. 1999.

[2] H. Wu *et al.*, "Silicon-based distributed voltage-controlled oscillators," *IEEE JSSC*, vol. 36, no. 3, Mar. 2001.

[3] J. Wood *et al.*, "Rotary travelling-wave oscillator arrays: a new clock technology," *IEEE JSSC*, vol. 36, no. 11, Nov. 2001.

[4] V. Chi, "Salphasic distribution of clock signals for synchronous systems," *IEEE Trans. Comp.*, vol. 43, pp. 597-602, May 1994.

[5] F. O'Mahony *et al.*, "10GHz clock distribution using coupled standing-wave oscillators," *IEEE ISSCC Dig. Tech. Papers*, pp. 428-429, Feb. 2003.

[6] D. Ham and W. Andress, "A circular standing wave oscillator," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004.

[7] W. Andress, *Theory and Techniques for Standing Wave Oscillators*, B.S. Thesis, Harvard University, 2004.

[8] D. Cheung *et al*, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," *IEEE ISSCC Dig. Tech. Papers,* pp. 396-397, Feb. 2003.

[9] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, pp. 329-330, Feb. 1966.