Digital Background Calibration in Pipelined ADCs Using Commutated Feedback Capacitor Switching

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***Abstract*—We propose a new digital background calibration method for capacitor mismatches in pipelined analog-to-digital converters (ADCs). It combines *commutated feedback capacitor switching* with a background digital correlation loop to extract capacitor mismatch information, which is subsequently used to correct errors caused by the mismatch. This is an all-digital technique requiring minimal extra digital circuits, and is applicable to both single-bit and multibit-per-stage architectures. Simulations with a 15-stage, 1.5-bit-per-stage pipelined ADC with capacitor mismatch of $\sigma = 0.25\%$ in each stage show that the technique improves signal-to-noise-distortion ratio from 62 dB (10 bits) to 94 dB (15.4 bits).**

***Index Terms*—Analog-to-digital converters (ADCs), calibration, digital background calibration, pipelined ADCs.**

I. Introduction

ONE primary consideration in the design of analog-to-digital converters (ADCs) is capacitor mismatch errors. Various calibration techniques to correct them have been developed in both analog and digital domains. Digital background calibration [4]–[17] is one class of such techniques.

In this paper, we propose a new technique for digital background calibration of capacitor mismatches in pipelined ADCs. The starting point of our work is *commutated feedback capacitor switching* (CFCS), originated from [1], [2]. This original work used CFCS to remove differential nonlinearity, and later, to effectively shape mismatch-induced spectra out of the signal band [3]. The contribution of the present work is to use CFCS in a new way, suited for digital background calibration: we use CFCS in cooperation with a background digital correlation loop to extract capacitor mismatch information, which we then use to correct the mismatch errors. This approach adds minimal digital cost.

Section II reviews the original CFCS technique of [1], [2], on which we build our calibration technique. Sections III–V describe our technique for 1-bit, 1.5-bit, and multibit-per-stage pipelined ADCs. Section VI presents simulations.

II. The Original CFCS Technique: Review

Let us consider a standard 1-bit-per-stage pipelined ADC. For simple exposition of CFCS, we assume capacitor mismatches only in the most-significant-bit (MSB) stage. Fig. 1(a) and (b) shows two different operational phases of the MSB stage. We represent the mismatches between the two, ideally the same capacitors, C_1 and C_2, with parameter Δ defined as $\Delta \equiv (C_1/C_2) - 1$. In the sampling phase [Fig. 1(a)], the ADC's input voltage $V_{\rm in}$ sampled and held on C_1 and C_2 is compared to voltage zero to make decision on the MSB, d_1. In the subsequent charge transfer phase [Fig. 1(b)], $V_{\rm REF}$ or $-V_{\rm REF}$ will be connected to C_1 according to d_1, and the total charge will be redistributed between C_1 and C_2, resulting in the following residue voltage $V_{\rm RES}$:

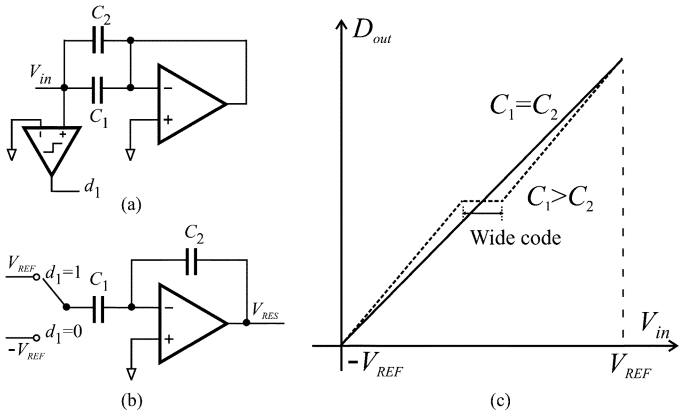

Fig. 1. (a) Sampling phase in the MSB stage in a 1-bit-per-stage pipelined ADC. (b) Charge transfer phase. (c) Overall transfer curves.

$$V_{\rm RES} = \begin{cases} (2+\Delta)V_{\rm in} + (1+\Delta)V_{\rm REF}, & \text{for } d_1 = 0 \\ (2+\Delta)V_{\rm in} - (1+\Delta)V_{\rm REF}, & \text{for } d_1 = 1. \end{cases} \quad (1)$$

$V_{\rm RES}$ is now an input to the following stage, which generates the second-significant bit, d_2. Repeating this procedure, $V_{\rm in}$ is converted to a set of digitized bits, $\{d_1, d_2, d_3, \ldots, d_N\}$ (N: total number of stages in the pipelined ADC). This set of bits is the digital output of the ADC, or alternatively, we may think of $D_{\rm out} \equiv -V_{\rm REF} + 2V_{\rm REF} \sum_{i=1}^{N} (d_i 2^{-i})$ as a representation of the ADC's digital output. Using (1), we can relate $D_{\rm out}$ to $V_{\rm in}$ via

$$D_{\rm out} = \begin{cases} (1+\Delta/2)V_{\rm in} + (\Delta/2)V_{\rm REF}, & \text{for } d_1 = 0 \\ (1+\Delta/2)V_{\rm in} - (\Delta/2)V_{\rm REF}, & \text{for } d_1 = 1. \end{cases} \quad (2)$$

We have omitted quantization noise terms to highlight capacitor mismatch effects.

Fig. 1(c) plots the ADC transfer curve, $D_{\rm out}$ versus $V_{\rm in}$, using (2). It is a straight line if $\Delta = 0$; for $\Delta \neq 0$, a discontinuity appears in the transfer curve, shown as wide code [1] in Fig. 1(c), causing differential nonlinearity (DNL).

Manuscript received February 21, 2008. First published June 10, 2008; current version published September 12, 2008. This work was supported by the National Science Foundation under Grant NSF-PHY-06–46094. This paper was recommended by Associate Editor G. Manganaro.

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Digital Object Identifier 10.1109/TCSII.2008.924369

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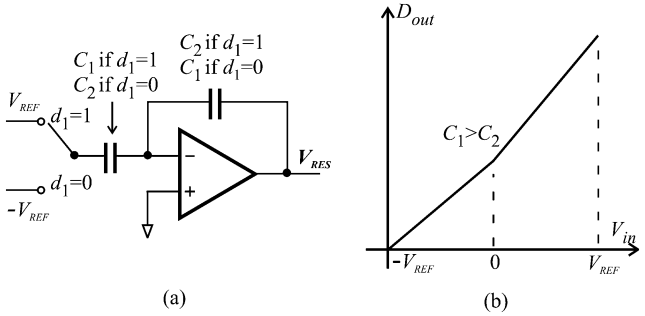

Fig. 2. CFCS [1], [2]. (a) Charge transfer phase. (b) Transfer curve.

To solve this DNL problem, CFCS was proposed and demonstrated in [1], [2]. CFCS is applied during the charge transfer phase, as shown in Fig. 2(a). If $d_1 = 0$, C_1 is selected as a feedback capacitor. If $d_1 = 1$, C_2 is selected as a feedback capacitor. The essence of CFCS is that the selection of the feedback capacitor in the charge transfer phase is based on d_1 determined in the prior sampling phase. CFCS alters the expression for the residue voltage of the MSB stage from (1) to the following:

$$V_{\rm RES} = \begin{cases} (2-\Delta)V_{\rm in} + (1-\Delta)V_{\rm REF}, & \text{for } d_1 = 0 \\ (2+\Delta)V_{\rm in} - (1+\Delta)V_{\rm REF}, & \text{for } d_1 = 1. \end{cases} \quad (3)$$

Subsequently, the ADC output $D_{\rm out}$ is related to $V_{\rm in}$ via

$$\begin{aligned} D_{\rm out} &= \begin{cases} (1-\Delta/2)V_{\rm in} - (\Delta/2)V_{\rm REF}, & \text{for } d_1 = 0 \\ (1+\Delta/2)V_{\rm in} - (\Delta/2)V_{\rm REF}, & \text{for } d_1 = 1 \end{cases} \\ &= V_{\rm in} + (\Delta/2)(|V_{\rm in}| - V_{\rm REF}). \end{aligned} \quad (4)$$

In the simplification into the last line, we have used the fact that $V_{\rm in} > 0$ for $d_1 = 1$ and $V_{\rm in} < 0$ for $d_1 = 0$. The ADC transfer curve, $D_{\rm out}$ versus $V_{\rm in}$, according to (4), is in Fig. 2(b). The curve discontinuity has now disappeared, removing DNL.

III. CFCS-Based Digital Background Calibration: 1-Bit-per-Stage Case

A. Basic Concepts

Our work in this paper builds up on CFCS of [1], [2]. In the present work, we use CFCS to extract the capacitor mismatch information, in conjunction with a background digital-correlation loop. The extracted mismatch information is subsequently used to calibrate out errors caused by the mismatch. This approach can improve ADC accuracy beyond what removal of only DNL can achieve.

The central idea of this work, extraction of capacitor mismatch information using CFCS, came from the realization that there are two ways of executing CFCS in 1-bit-per-stage pipelined ADCs. We already discussed one way in the previous section: we selected C_1 as a feedback capacitor for $d_1 = 0$ and C_2 as a feedback capacitor for $d_1 = 1$ [Fig. 2(a); redrawn in Fig. 3(a)]. We call this specific CFCS execution, which led to (4), CFCS-A. The other way is to select C_2 as a feedback capacitor for $d_1 = 0$ and to select C_1 as a feedback capacitor for $d_1 = 1$ [Fig. 3(b)]. We refer to this CFCS execution as CFCS-B, for which $V_{\rm RES}$ is given by

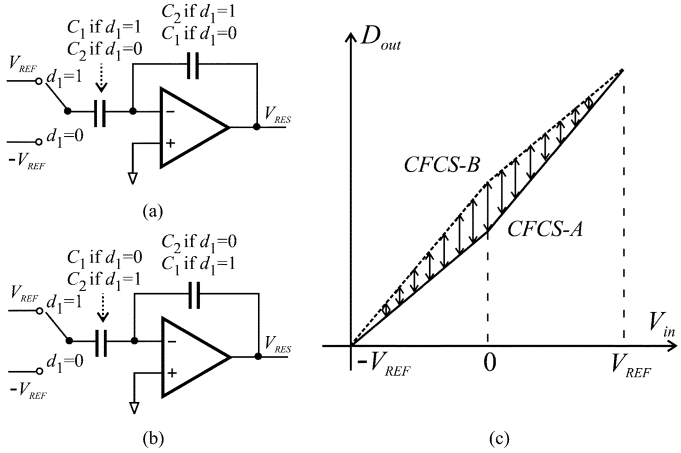

Fig. 3. (a) CFCS-A. (b) CFCS-B. (c) ADC transfer curves for CFCS-A and CFCS-B, for $\Delta > 0$.

$$V_{\rm RES} = \begin{cases} (2+\Delta)V_{\rm in} + (1+\Delta)V_{\rm REF}, & \text{for } d_1 = 0 \\ (2-\Delta)V_{\rm in} - (1-\Delta)V_{\rm REF}, & \text{for } d_1 = 1 \end{cases} \quad (5)$$

and accordingly, $D_{\rm out}$ is related to $V_{\rm in}$ via

$$D_{\rm out} = V_{\rm in} - (\Delta/2)(|V_{\rm in}| - V_{\rm REF}). \quad (6)$$

As evident from (4) and (6), CFCS-A and CFCS-B lead to different ADC transfer characteristics: see Fig. 3(c). For the same analog input $V_{\rm in}$, the digital output $D_{\rm out}$ of CFCS-A is always smaller than CFCS-B for $\Delta > 0$, and *vice versa* for $\Delta < 0$. The distance between the two transfer curves is proportional to Δ, as we can see by subtracting (6) from (4):

$$D_{{\rm out},A} - D_{{\rm out,B}} = \Delta \cdot (|V_{\rm in}| - V_{\rm REF}) \quad (7)$$

where subscripts A and B indicate use of CFCS-A and CFCS-B, respectively. Now Δ may be expressed as

$$\Delta \approx \frac{D_{{\rm out},A} - D_{{\rm out},B}}{|D_{{\rm out},A}| - V_{\rm REF}}. \quad (8)$$

In going from (7) to (8), we approximated $|V_{\rm in}|$ with $|D_{{\rm out},A}|$ to express Δ in terms of digital quantities available at the ADC output. We may alternatively replace $|V_{\rm in}|$ with $|D_{{\rm out},B}|$. The difference between $|D_{{\rm out},A}|$ and $|D_{{\rm out},B}|$ in the denominator adds only a second-order effect in the expression of Δ. Equation (8) shows that by measuring the distance $D_{{\rm out},A} - D_{{\rm out},B}$ between the transfer curves for CFCS-A and CFCS-B for any input $V_{\rm in}$, we can in principle extract the capacitor mismatch information, Δ, which we can subsequently use to calibrate out errors caused by the mismatch.

B. Implementation

In reality, we cannot simultaneously obtain $D_{{\rm out},A}$ and $D_{{\rm out},B}$ for a given input $V_{\rm in}$. We could do so if we had two identical ADCs, and operated one with CFCS-A and the other with CFCS-B, but such an arrangement is impossible. Therefore, extraction of Δ directly using (8) is not feasible.

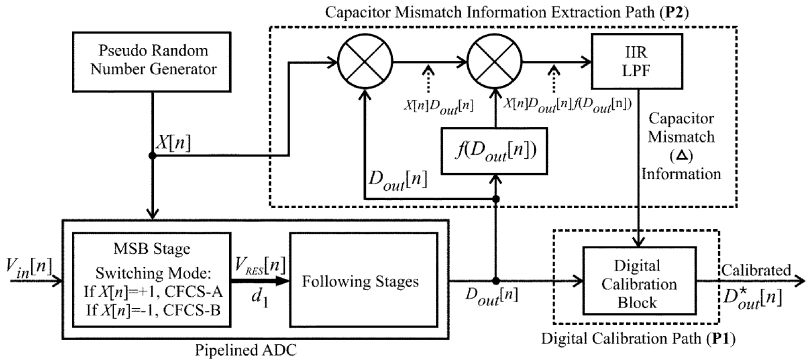

Fig. 4. Architecture and discrete-time signal processing for our digital background calibration.

We can instead obtain a time-averaged version of (7) or (8) to extract Δ. This can be done in a given ADC first by randomly choosing one CFCS mode between CFCS-A or CFCS-B with equal probability for each input sample, then by creating a data sequence consisting of the resulting ADC outputs but with each output multiplied by 1 if CFCS-A was used and by -1 if CFCS-B was used, and then by time-averaging (low-pass filtering) the data sequence. This procedure to extract Δ can be executed using a background digital correlation loop shown in Fig. 4.

Let us take a close look at the discrete-time processing in Fig. 4. For simplicity, we continue to assume capacitor mismatches only in the MSB stage, and hence, in Fig. 4, the calibration is performed only in the MSB stage. Switching between CFCS-A and CFCS-B in the MSB stage is controlled by a pseudorandom variable $X[n]$, which assumes $+1$ and -1 with equal probability. When $X[n] = 1$, CFCS-A is executed, and ADC output $D_{\text{out},A}$ of (4) results; when $X[n] = -1$, the MSB stage executes CFCS-B, yielding ADC output $D_{\text{out},B}$ of (6). We can combine (4) and (6) into one equation, noting $X[n] = 1$ for CFCS-A and $X[n] = -1$ for CFCS-B:[1]

$$D_{\text{out}}[n] = V_{\text{in}}[n] + X[n] \cdot (\Delta/2)\,(|V_{\text{in}}[n]| - V_{\text{REF}})\,. \quad (9)$$

This pre-calibration ADC output with the error term, $X[n] \cdot (\Delta/2)(|V_{\text{in}}[n]| - V_{\text{REF}})$, which we aim to calibrate out eventually, is now separated into calibration path **P1** and capacitor mismatch information extraction path **P2** [Fig. 4]. We will focus on **P2** for now.

In **P2**, $D_{\text{out}}[n]$ is first multiplied by $X[n]$, is subsequently multiplied by a certain function of $D_{\text{out}}[n]$, $f(D_{\text{out}}[n])$, and then goes through the discrete-time infinite-impulse response (IIR) low-pass filter (LPF). For 1-bit-per-stage pipelined ADCs, we use $f(D_{\text{out}}[n]) = 1$. The utility of $f(D_{\text{out}}[n])$ will become clear in the next two sections when we discuss the calibration of 1.5-bit-per-stage and multibit-per-stage architectures.

The signal processing described above yields the following signal at the input of the IIR LPF of Fig. 4:

$$X[n]D_{\text{out}}[n] = X[n]V_{\text{in}}[n] + \frac{\Delta}{2}\,(|V_{\text{in}}[n]| - V_{\text{REF}})\,. \quad (10)$$

[1]To be rigorous, $V_{\text{in}}[n - N]$ can be used instead of $V_{\text{in}}[n]$ to account for the time delay in the pipelined ADC, but such a distinction is unnecessary in understanding the essence of our scheme.

The IIR LPF outputs a dc component (time average) of the input signal of (10). Since $X[n]$ is a pseudorandom signal taking ± 1 and is not correlated with $V_{\text{in}}[n]$, the dc component of the first term of (10) is zero. In contrast, the second term of (10) is always positive or negative, for $|V_{\text{in}}[n]| \le V_{\text{REF}}$, and has a nonzero dc component. Therefore, at the output of the IIR LPF we attain

$$\overline{X[n]D_{\text{out}}[n]} = \frac{\Delta}{2}(\overline{|V_{\text{in}}[n]|} - V_{\text{REF}}). \quad (11)$$

where the overlines signify dc components or time averaging. Note (11) is a time-averaged version of (7). From (11), we can express Δ as

$$\Delta \approx 2 \cdot \frac{\overline{X[n]D_{\text{out}}[n]}}{\overline{|D_{\text{out}}[n]|} - V_{\text{REF}}}. \quad (12)$$

where we approximated $\overline{|V_{\text{in}}[n]|}$ with $\overline{|D_{\text{out}}[n]|}$ in going from (11) to (12): the difference between $\overline{|V_{\text{in}}[n]|}$ and $\overline{|D_{\text{out}}[n]|}$ in the denominator on the right hand side of (12) produces only a second-order effect in the Δ expression. Now in (12), Δ is expressed in terms of quantities that we can explicitly measure and know. First, $\overline{|D_{\text{out}}[n]|}$ in the denominator on the right-hand side of (12) can be measured by low-pass filtering the pre-calibration ADC output $D_{\text{out}}[n]$. Second, the numerator on the right-hand side of (12) is what we measure at the output of the IIR LPF. Therefore, (12), as a result of the background digital correlation procedure of Fig. 4 in conjunction with CFCS, is the ultimate equation that quantitatively informs on the capacitor mismatch, Δ. Note that (12) is the time-averaged version of (8).

Once Δ is thus determined, we can use it to calibrate out the error term in the pre-calibration ADC output $D_{\text{out}}[n]$ of (9) in a straightforward fashion using a digital calibration block in **P1** of Fig. 4. The basic operation that it performs is

$$\begin{aligned} D^*_{\text{out}}[n] &= D_{\text{out}}[n] - X[n] \cdot (\Delta/2)\,(|D_{\text{out}}[n]| - V_{\text{REF}}) \\ &\approx V_{\text{in}}[n] \end{aligned} \quad (13)$$

where what is subtracted from $D_{\text{out}}[n]$ in the first line is what we now know (as Δ has been determined). In obtaining the second line using (9) for $D_{\text{out}}[n]$, we omitted second-order effects. In (13), $D^*_{\text{out}}[n]$ represents the corrected digital output [Fig. 4].

Before concluding this section, we remark that quantization noise has been omitted in the foregoing calculation to highlight the capacitor mismatch effect, but this seemingly incomplete

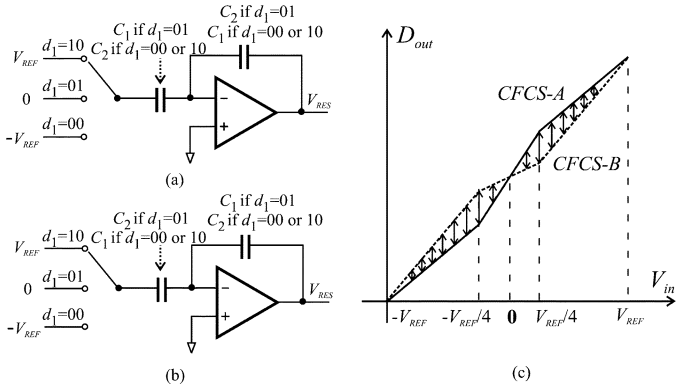

Fig. 5. 1.5-bit-per-stage case. (a) CFCS-A. (b) CFCS-B. (c) Transfer curves for CFCS-A and CFCS-B for $\Delta > 0$.

calculation does not make the extraction of the mismatch information Δ, or (12), any less accurate. If we had carried out the calculation including quantization noise $e[n]$, we would have had an additional term $\overline{X[n]e[n]}$ in the numerator of (12), but the time average of $e[n]$ sufficiently dithered by $X[n]$ is a significantly reduced quantity, which may be ignored. In contrast, the correction of the digital output using (13) is affected by quantization noise, for there is no averaging involved in this final step of calibration. As a result, final accuracy will be slightly less than the target resolution, as seen in simulations later. This inaccuracy problem arising in the final correction step, intrinsic in all digital calibration schemes, can be addressed by adding a couple of bits at the back end at low cost, although we have not taken this generic step, for it is tangential to our goal of demonstrating the new calibration method.

IV. CFCS-Based Digital Background Calibration: 1.5-Bit-per-Stage Case

Our calibration technique can be applied to 1.5-bit-per-stage pipelined ADCs, which is the topic of this section. We will continue to assume capacitor mismatches only in the MSB stage. We denote the MSB stage's digital decision again as d_1, which now assumes one of 00, 01, and 10. As shown in Fig. 5, there are two capacitors C_1 and C_2 in the MSB stage, whose mismatch is again represented by $\Delta \equiv (C_1/C_2) - 1$.

The starting point, as in the 1-bit-per-stage case, is realizing that there are two different ways of executing CFCS. One way (CFCS-A) is to select C_1 as a feedback capacitor when $d_1 = 01$ and to select C_2 as a feedback capacitor when $d_1 = 00$ or 10 [Fig. 5(a)]. The other way (CFCS-B) is to select C_2 as a feedback capacitor when $d_1 = 01$ and to select C_1 as a feedback capacitor when $d_1 = 00$ or 10 [Fig. 5(b)]. For CFCS-A, $D_{\text{out},A}$ is related to V_{in} through

$$D_{\text{out},A} = \begin{cases} (1-\Delta/2)V_{\text{in}} - (\Delta/2)V_{\text{REF}}, & d_1 = 00 \\ (1+\Delta/2)V_{\text{in}}, & d_1 = 01 \\ (1-\Delta/2)V_{\text{in}} + (\Delta/2)V_{\text{REF}}, & d_1 = 10. \end{cases} \quad (14)$$

For CFCS-B, $D_{\text{out},B}$ is related to V_{in} via

$$D_{\text{out},B} = \begin{cases} (1+\Delta/2)V_{\text{in}} + (\Delta/2)V_{\text{REF}}, & d_1 = 00 \\ (1-\Delta/2)V_{\text{in}}, & d_1 = 01 \\ (1+\Delta/2)V_{\text{in}} - (\Delta/2)V_{\text{REF}}, & d_1 = 10. \end{cases} \quad (15)$$

Equations (14) and (15) show that as in the 1-bit-per-stage case, CFCS-A and CFCS-B result in two different transfer curves, as shown in Fig. 5(c), and the distance between the two curves is proportional to Δ. Just like in the 1-bit-per-stage case, we are now to extract Δ, by measuring the distance using the background digital correlation architecture of Fig. 4.

Note, however, that unlike the 1-bit-per-stage case where the transfer curve for CFCS-A is always below that for CFCS-B [Fig. 3(c); $\Delta > 0$], the two transfer curves for CFCS-A and CFCS-B in the 1.5-bit-per-stage case have a crossover at $V_{\text{in}} = D_{\text{out}} = 0$ and $D_{\text{out},A}[n] > D_{\text{out},B}[n]$ for $V_{\text{in}}[n] > 0$ but $D_{\text{out},A}[n] < D_{\text{out},B}[n]$ for $V_{\text{in}}[n] < 0$ [Fig. 5(c); $\Delta > 0$]. Therefore, if we use $f(D_{\text{out}}[n]) = 1$ as in the 1-bit-per-stage case, the resultant signal $X[n]D_{\text{out}}[n]$ ($X[n] = 1$ for CFCS-A; $X[n] = -1$ for CFCS-B) at the input of the IIR LPF of Fig. 4 will be time-averaged to zero at the output of the LPF, no matter what the value of Δ is. Therefore, with $f(D_{\text{out}}[n]) = 1$, we cannot extract Δ.

This problem can be solved by using $f(D_{\text{out}}[n])$ specifically defined, for the 1.5-bit-per-stage case, as the following:

$$f(D_{\text{out}}[n]) = \begin{cases} +1, & \text{if } D_{\text{out}}[n] \le 0 \\ -1, & \text{if } D_{\text{out}}[n] > 0. \end{cases} \quad (16)$$

With this $f(D_{\text{out}}[n])$, $D_{\text{out}}[n]f(D_{\text{out}}[n])$ of CFCS-A will be always smaller than that of CFCS-B for any given $V_{\text{in}}[n]$, and hence the input to the IIR LPF in Fig. 4, $X[n]D_{\text{out}}[n]f(D_{\text{out}}[n])$, will be time-averaged to a nonzero value that is proportional to Δ. This way we extract the capacitor mismatch information in the 1.5-bit-per-stage pipelined ADC.

V. CFCS-Based Digital Background Calibration: Multibit-Per-Stage Case

Our background calibration technique can be easily generalized from 1-bit-per-stage and 1.5-bit-per-stage cases to m-bit-per-stage or $(m+0.5)$-bit-per-stage cases (typical values for m are 1, 2, and 3). There are total 2^m capacitors in each stage, and we again assume capacitor mismatches only in the MSB stage for simplicity and focus on the MSB stage. We denote the capacitors in the MSB stage as $C_1, C_2, C_3, \ldots, C_{2^m}$ and represent the capacitor mismatch between C_k and C_{k+1} as $\Delta_k \equiv (C_{k+1}/C_k) - 1$ where $k = 1, 2, 3 \ldots, (2^m - 1)$. Once every Δ_k is extracted, we can calibrate out errors brought by all mismatches.

We use the procedure of Fig. 4 to extract Δ_k. We first define two CFCS execution modes, which we call CFCS-A$_k$ and CFCS-B$_k$. In CFCS-A$_k$, we select C_k as a feedback capacitor if d_1 is even, and select C_{k+1} as a feedback capacitor if d_1 is odd. In CFCS-B$_k$, we select C_{k+1} as a feedback capacitor if d_1 is odd, and select C_k as a feedback capacitor if d_1 is even. $f(D_{\text{out}})$ is set at 1 at $D_{\text{out}} = V_{\text{in}} = -V_{\text{REF}}$ and continues to be 1 with increasing V_{in} until there is a crossover between the transfer curves of CFCS-A$_k$ and CFCS-B$_k$: at the crossover, $f(D_{\text{out}}[n])$ becomes -1 and remains to be -1 until the next crossover. This procedure is repeated to completely determine $f(D_{\text{out}}[n])$. This ensures that $D_{\text{out}}[n]f(D_{\text{out}}[n])$ of CFCS-A$_k$ is always smaller (larger) than CFCS-B$_k$ for $\Delta_k > 0$ ($\Delta_k < 0$). From the output of the IIR LPF, we extract Δ_k.

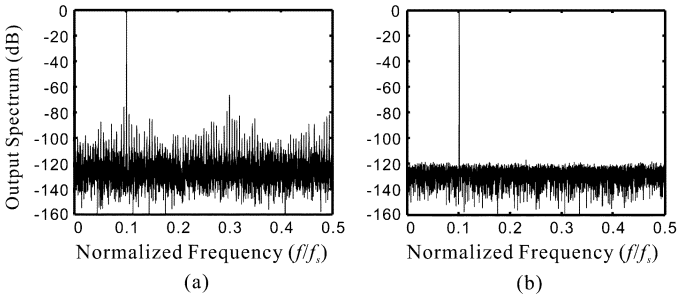

Fig. 6. Simulated output spectra. (a) Pre-calibration. (b) Post-calibration.

The overall calibration algorithm can be summed up as follows, for each input sample (for each time index n).

1) Select k and decide which Δ_k is to be extracted, using a pseudorandom signal $X_{\text{cap}}[n] = 1, 2, 3 \ldots, (2^m - 1)$ (equal probability).
2) Select which CFCS mode to use between CFCS-A$_k$ and CFCS-B$_k$, according to another pseudorandom signal $X_{\text{mode}}[n] = \pm 1$ (equal probability).
3) Let $X_{\text{mode}}[n] D_{\text{out}}[n] f(D_{\text{out}}[n])$ go through the kth LPF. From the output, Δ_k is extracted.
4) Using this Δ_k, perform digital calibration).

VI. Simulation

We test our CFCS-based digital background calibration, using behavioral simulations in MATLAB. A 16-bit pipelined ADC consisting of 15 1.5-bit stages is modeled, and random capacitor mismatches of $\sigma = 0.25\%$ are assumed in each stage. First 6 stages are calibrated in parallel using the proposed technique. Each of the stages has its own LPF and pseudorandom generator with a period of 2^{14}. Fig. 6 shows the simulated output spectra of the pipelined ADC for a full-swing sine wave input, whose frequency is $1/\sqrt{101}$ of the sampling frequency: we chose this irrational number so that the signal is always sampled at different phases to avoid periodicity. The number of samples we used is 2^{14}. The window we used is Kaiser Window $\beta = 20$ with window length 2^{14}.

Fig. 6(a) is the output spectrum in the absence of the digital background calibration. We see appreciable harmonics generated by capacitor mismatches. When our digital background calibration is in force, the output spectrum of Fig. 6(b) is obtained. Not only are the large harmonics eliminated, but the noise floor due to high order harmonics is also significantly reduced. Quantitatively, the calibration increases the spurious-free-dynamic-range (SFDR) from 70 dB to 120 dB, and the signal-to-noise-and-distortion-ratio (SNDR) from 62 dB (10 bits) to 94 dB (15.4 bits), clearly demonstrating the validity of the proposed technique. The perfect 16-bit resolution was not achieved due to two main reasons: firstly, the calibration was performed only for the first 6 stages; secondly, although the extracted value of Δ is precise to the first order, quantization noise compromises the correction of the digital output using the extracted Δ, as mentioned at the end of Section III.

VII. Conclusion

We introduced a new digital background calibration technique for capacitor mismatches in pipelined ADCs. Its novelty is combining two known techniques, CFCS [1], [2] and a digital correlation loop, to extract capacitor mismatch information. This approach is applicable to single- and multibit-per-stage cases. The cost of implementing our technique is low: only shift registers, discrete-time LPF, and simple combinational logic are needed in the background calibration loop.

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