A 2.9-mW 11-b 20-MS/s Pipelined ADC with Dual-Mode-Based Digital Background Calibration

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***Abstract*—We report an 11-b 20-Ms/s pipelined ADC in 0.18-μm CMOS with a novel dual-mode-based digital background calibration method that altogether corrects errors caused by gain insufficiency, gain nonlinearity, and capacitor mismatches. The calibration enables an intentional use of low-gain single-stage op amps instead of conventional high-gain multi-stage op amps, with which we achieve a total ADC power dissipation of 2.9 mW and a short convergence time of 10^5. The calibration improves the SNDR from 45 dB to 60 dB, and the SFDR from 50 dB to 86 dB. The figure-of-merit is 174 fJ/conversion-step.**

I. Introduction

The most power-hungry element in traditional pipelined ADCs is the op-amp. For low power design of pipelined ADCs, various designs to circumvent the op-amp power consumption have been investigated. One approach has received particular attention. In this approach, conventional high-gain op-amps are replaced by low-gain amplifiers that dissipate much less power, and substantial conversion errors caused by low-gain amplifiers are corrected using digital background calibration techniques [1]–[7].

This paper reports a low-power (2.9 mW) 11-b 20-Ms/s pipelined ADC, which is designed in the spirit of this approach. We use simple single-stage telescopic op amps to substantially save power. To correct conversion errors caused by gain insufficiency and nonlinearity arising from low-gain op amps as well as capacitor mismatches, we devise a new dual-mode-based digital background calibration technique. This calibration technique, which is the key design contribution of this paper, works by operating *one* ADC in two configurations. These two modes are so arranged that their digital outputs differ in the presence of gain insufficiency and nonlinearity, and capacitor mismatches. The output difference is measured by randomly choosing one of the two modes at each sampling clock and digitally correlating the resulting digital output sequence. The measured output difference, which represents ADC errors, is used to remove the errors. In experiments with the 0.18-μm CMOS ADC prototype, the background calibration improves SNDR from 45 dB to 60 dB, and SFDR from 50 dB to 86 dB. The figure-of-merit (FOM) is 174 fJ/conversion-step after calibration.

There are previous background calibration techniques that correct gain nonlinearity as well as insufficient gain and capacitor mismatches [4]–[7]. [4] also used two modes, measuring their output differences at two fixed input values. In contrast, we measure output differences averaged over input signal ranges, and with new circuit topologies for the two modes. The result is less susceptibility to comparator offsets and faster convergence. Unlike [5], the injection of the input dithering signal is unnecessary, thus the available input range is not reduced and the convergence is much faster. Also, different from [6], [7], extra time slots for test signals are not needed, and hence, the frequency of the input is not limited.

II. Dual-Mode Based Background Calibration

A. Main Calibration Algorithm

A 1.5-b-per-stage pipelined ADC is chosen as a demonstrational vehicle. For brevity, we assume nonidealities only in the 1st stage, although our actual implementation expands the principle to subsequent stages.

Fig. 1(a) shows the sampling phase. The topology is standard, except three extra comparators are used. The total of five comparators compare a sampled input, V_{in}, to five levels, 0, $\pm 1/4$, $\pm 1/2$, to locate it in one of the six input regions ①∼⑥. It is in the subsequent charge transfer phase that two modes, which we call $Mode\text{-}A$ and $Mode\text{-}B$, are used. In $Mode\text{-}A$ [Fig. 1(b)], capacitor C_1 is split into two sub-capacitors, $C_1/3$ and $2C_1/3$. $C_1/3$ is connected to ground; $2C_1/3$ is connected to one of the three reference voltages, 0, $\pm 3V_{REF}/2$, depending on which of regions ①∼⑥ contains the sampled input. The residue curve for $Mode\text{-}A$ is the same as that of the standard 1.5-b stage. In $Mode\text{-}B$ [Fig. 1(c)], C_1 is again split into two sub-capacitors, $C_1/3$ and $2C_1/3$, but these sub-capacitors are connected to the three references in a different way. The residue curve is the same as that of the standard 2-b stage (with 1-b redundancy).

The overall ADC input-output transfer curve for each mode is shown in Fig. 2. The $Mode\text{-}A$ transfer curve is similar to that of the 1.5-b stage, with two regions of missing codes at $\pm 1/4$. The $Mode\text{-}B$ transfer curve is similar to that of the 2-b stage, with three regions of missing codes at 0 and $\pm 1/2$. All the gaps, caused by the missing codes, have the same length, regardless of the mode used or gap position. The gaps are the combined effect of the gain insufficiency and nonlinearity, and C_1-C_2 capacitor mismatches. The curvature in each transfer curve is a manifestation of the gain nonlinearity. Thus, the gaps and curvature in the transfer curves represent ADC errors caused by the nonidealities. Once the gap length and curvature are extracted, the ADC errors can be corrected.

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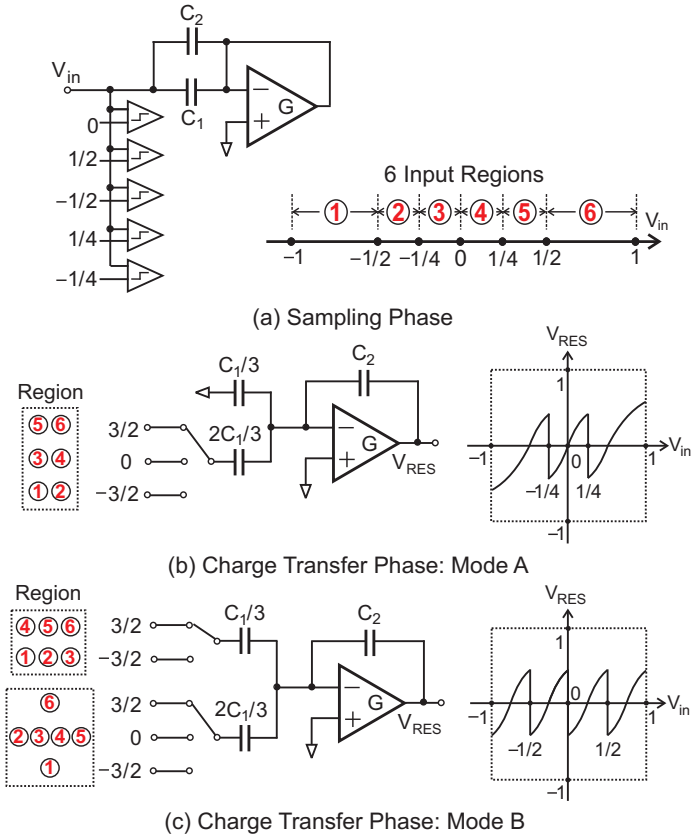

Fig. 1. Two operation modes.

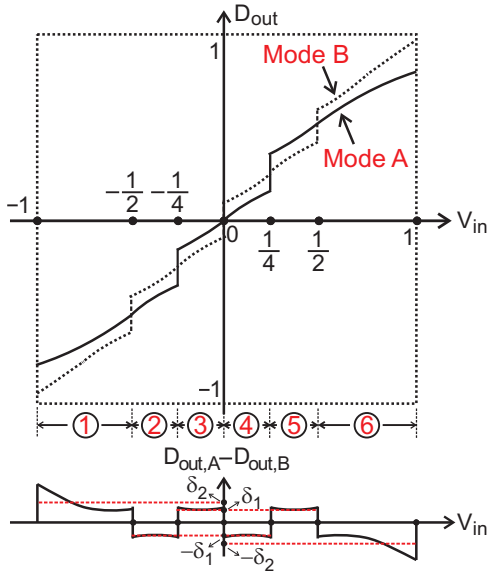

Fig. 2. Transfer curves for the two modes.

The gap length and curvature can be extracted from the output difference between the two modes, which is shown at the bottom of Fig. 2. The output difference averaged over any one of regions ②, ③, ④, and ⑤ has the same magnitude, which we call δ_1; the output difference averaged over ① or ⑥ has the same magnitude, which we call δ_2. Two key observations by inspection of the figure are: 1) δ_1 and δ_2 are proportional to the gap length; 2) $\delta_2 > \delta_1$, because the residue gain nonlinearity causes larger errors at larger residue voltages, and hence, the disparity between δ_1 and δ_2 reflects the gain nonlinearity, or, the curvature. Therefore the gap length and curvature can be extracted from the averaged output differences, δ_1 and δ_2.

We measure δ_1 and δ_2 using digital background correlation [Fig. 3]. Pseudo-random number R, assuming ± 1, selects one of the two modes. Correlation of the ADC output D_{out} with R, followed by a low-pass-filter (LPF), produces the averaged output differences. The demultiplexer (DEMUX) controlled by the 1st-stage comparator decision d_1 is to obtain the averaged output difference in each of the six input regions, ①∼⑥. The six averaged output differences, among which four have the magnitude δ_1 and two have the magnitude δ_2, are used in the coefficient estimation block to compute the gap length and curvature. These are used in the correction block to produce an error-free output, D^*_{out}.

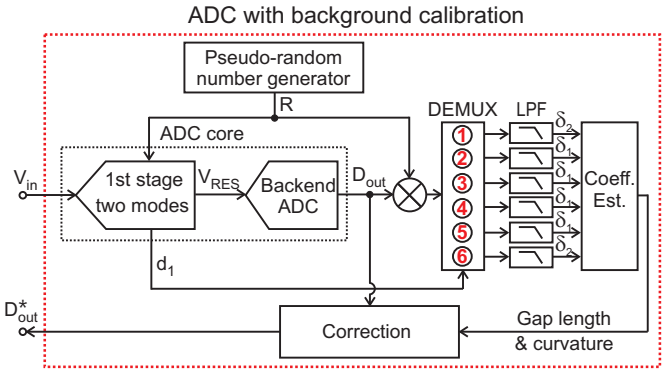

Fig. 3. Block diagram for the dual-mode-based background calibration.

While δ_1 can always be extracted, δ_2 cannot be obtained if the input is small and does not reach regions ① and ⑥. Under such condition, the algorithm only corrects gap errors, and does not correct curvature errors. Nevertheless, the algorithm still works well for a target ENOB $\leq$ 12b as in our design, because the curvature error due to gain nonlinearity is not appreciable for the small input.

B. Practical Design Considerations

As compared to the standard 1.5-b stage, our dual-mode arrangement adds three extra comparators [Fig. 1(a)], which dissipate power and also load the op amp to increase its power consumption. However, this extra power consumption can be made insignificant. First, comparator offsets as large as $\pm 1/4$ are tolerated, thus, the comparators can be designed as dynamic latches with power consumption negligible compared to op amps. Second, small input transistors of the dynamic latches keep the loading on the op amp small. Hence, the extra power consumption can be made dominated over by the power saving due to the intentional use of the low gain op amps, leading to substantially reduced overall power budget.

Although a non-standard set of reference voltages ($\pm V_{REF}/4$, $\pm V_{REF}/2$, and $\pm 3V_{REF}/2$) is used, it does

not cause implementation issues. First, only $\pm 3V_{REF}/2$ used during charge transfer needs to be accurate, for our calibration is insensitive to small deviation in comparator references. Thus, the total number of accurate references needed in our design is the same as in the conventional design. Second, although the use of $3V_{REF}/2$ limits the input range of $2V_{REF}$ to $4V_{DD}/3$ because $3V_{REF}/2$ must be less than V_{DD}, this does not necessarily mean a smaller input range for our scheme, since the actual input range limited by other circuit nonidealities is often smaller than $4V_{DD}/3$, such as in [1]–[7], [9], [10]. Also, in our implementation with $V_{DD} = 1.8$ V, $4V_{DD}/3 = 2.4$ V, but the actual input range is 2 V V_{pp}, which is limited by the op amp's nonlinearity.

Our main calibration (Sec. II-A) corrects errors brought by C_1-C_2 mismatch, but it cannot handle the sub-capacitor mismatch between $C_1/3$ and $2C_1/3$ [Figs. 1(b)/(c)]. To correct this sub-capacitor mismatch, an auxiliary background calibration [Fig. 4] similar to [8] is added. We use three $C_1/3$ capacitors for C_1 [Fig. 4]. The $C_1/3$–$2C_1/3$ pair during each charge transfer phase is formed by randomly selecting two of the three $C_1/3$ capacitors for $2C_1/3$ according to a random number S. S is sent to a separate correlator, to estimate mismatches among the three $C_1/3$ capacitors. In this way, the auxiliary calibration runs in parallel without disturbing the main dual-mode calibration.

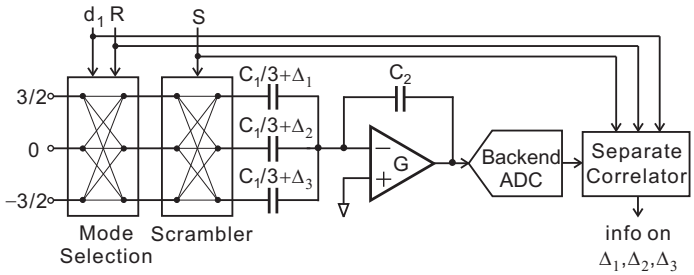

Fig. 4. Block diagram for the auxiliary digital background calibration for sub-capacitor mismatches.

III. Prototype ADC Design

An 11-b 20-Ms/s pipelined ADC [Fig. 5] is designed in 0.18-μm CMOS. It consists of 11 1.5-b stages and a backend 3-b flash ADC. Out of the 14 bits of raw data, the 3 least significant bits are used for calibration purpose and are truncated in the final digital output. The 1st 5 stages execute the calibration. Each stage uses a single-stage telescopic op amp with only 50-dB gain. Power saving stems mainly from the use of the single-stage op amps. Additional measures to further reduce power are: 1) the 1st 5 stages are consecutively halved in size, while the remaining stages have the same size as the 5th stage; 2) the op amps are powered off during sampling phase. Since the power-on speed of the single-stage op amp is fast ($<$ 200 ps), almost ideal 50% power reduction is attained; 3) the op-amp input transistors are biased with minimal overdrive to maximize g_m efficiency; 4) we obviate the use of a dedicated S/H by moving 1st stage comparators to the op amp output as in [9], [10].

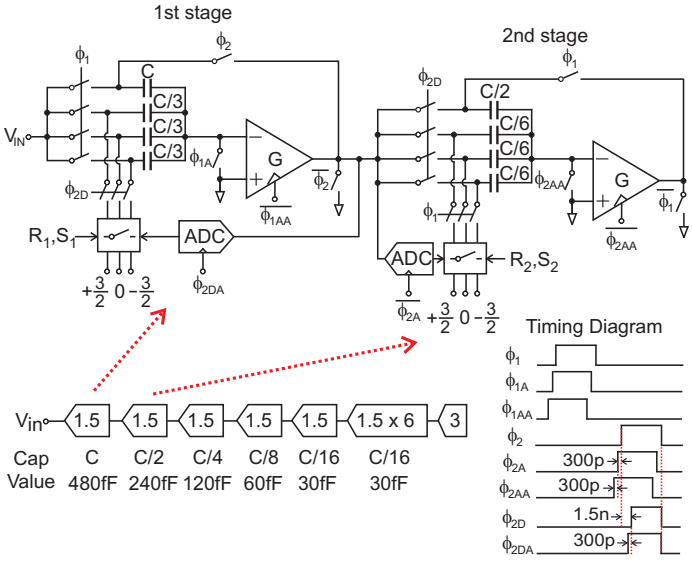

Fig. 5. ADC architecture, timing diagram, and schematics of 1st 2 stages.

IV. Experimental Results

The die micrograph is in Fig. 6. All analog circuits are implemented on chip. The active area excluding the output driver is 0.18 mm^2. The input range is 2 V V_{pp}. The sampling rate is 20.48 Ms/s. The real-time mode switchings are done using 5 pseudo-random number sequences, produced by linear feedback shift registers implemented on the PCB. The resulting raw digital output sequence from the ADC, acquired by a logic analyzer, goes through the digital computation of Fig. 3 (correlation, coefficient estimation, and correction) in a PC to yield calibrated digital outputs as is done in [3], [7].

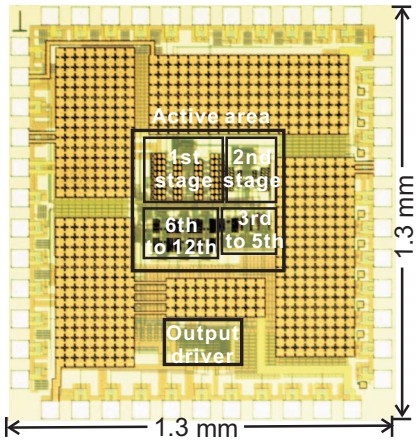

Fig. 6. Die photo.

Figs. 7 and 8 show the measured INL and output spectra before and after background calibration. Before calibration, INL, DNL, SNDR, and SFDR are $+15.4/-16.6$ LSB, $+1.3/-1.0$ LSB, 45 dB, and 50 dB, respectively. After calibration, INL, DNL, SNDR, and SFDR are improved to $+0.5/-0.5$ LSB, $+0.4/-0.4$ LSB, 60 dB, and 86 dB. Fig. 9 shows measured post-calibration SNDR and SFDR with varying input

frequencies and amplitudes. The background calibration was performed at each frequency and each amplitude.

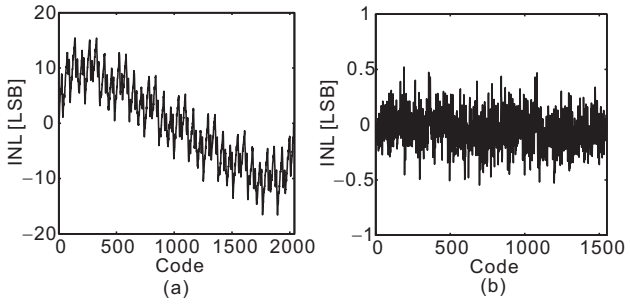

Fig. 7. Measured INL: (a) before calibration (b) after calibration.

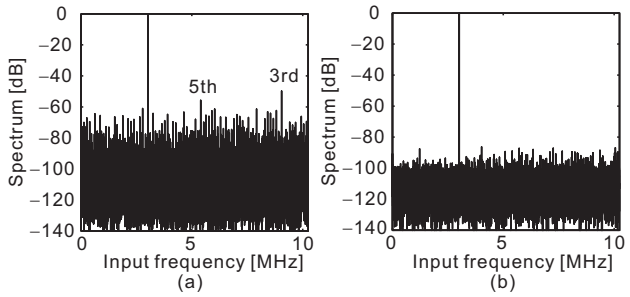

Fig. 8. Measured output spectra: (a) before calibration; (b) after calibration.

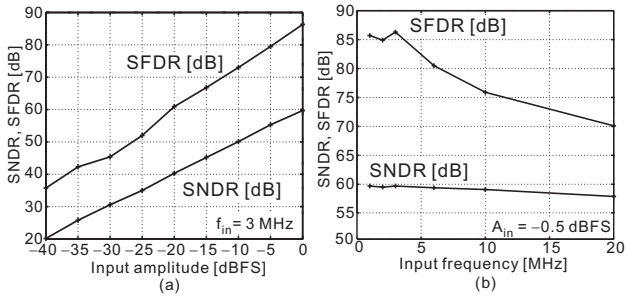

Fig. 9. Measured post-calibration SNDR and SFDR with: (a) varying input frequencies; (b) varying input amplitudes.

The measured required number of samples for convergence is 10^5, which is several orders of magnitude smaller than the state-of-the-art, e.g., 10^8 for [4] and 10^9 for [5]. This fast convergence speed allows the proposed technique to track op-amp gain variations much more quickly.

The measured on-chip power drawn from the analog power supply is 0.7 mW, dominated by op amps. The measured on-chip power drawn from the digital power supply (where switch drivers, clocking circuits, comparators, and logic gates are connected) is 1.6 mW, dominated by switch drivers. The digital tasks performed in the PC would require about 90,000 transistors, and assuming, conservatively, 50% of them are switched at each clock cycle, they would consume about 0.6 mW. Including this, the entire ADC consumes 2.9 mW. The corresponding FOM is 174 fJ/conversion-step.

Tab. I compares our work to recent experimental pipelined ADC works with digital background calibration. Our design has the best FOM among them. Such a comparison needs to be interpreted with caution, given different fabrication technologies and integration levels. Nonetheless, the performance suggests the efficacy of our design.

TABLE I
PERFORMANCE COMPARISON

Ref.	SNDR [dB]	SFDR [dB]	f_s [Ms/s]	Power [mW]	FOM [pJ/step]
[1]	72	90	40	400	3.07
[2]	70.2	80.9	20	231	4.37
[3]	60	70	45	81	2.20
[4]	68.2	76	75	314	1.99
[5]	69.8	85	100	130	0.51
[6]	72.6	84.5	80	755	2.71
[7]	61.5	N/A	200	186	0.96
Ours	60	86	20	2.9	0.17

V. SUMMARY

An 11-b 20-Ms/s pipelined ADC in 0.18-μm CMOS achieved 60 dB SNDR at 2.9 mW. The corresponding FOM is 174 fJ/conversion-step. The key design aspect is the new dual-mode-based digital background calibration technique that corrects the errors collectively caused by gain insufficiency, gain nonlinearity, and capacitor mismatches. Owing to this calibration, we were able to intentionally use low-gain single-stage op amps instead of conventional high-gain multi-stage op amps, which was the key to the low power dissipation of the ADC and the resulting low FOM.

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